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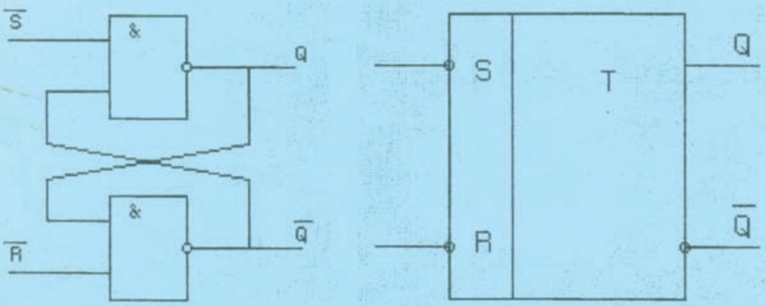
INTEGRATED CIRCUITRY



Vinnitsa VNTU 2005

Міністерство освіти і науки України
Вінницький національний технічний університет

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ІНТЕГРАЛЬНА СХЕМОТЕХНІКА

Затверджено Вченою радою Вінницького національного технічного університету як навчальний посібник для студентів спеціальності 7.091401– „Системи управління і автоматики”.

Протокол №4 від 27 листопада 2003 року.

Вінниця ВНТУ 2005

УДК 621.31
К 89

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Рекомендовано до видання Вченою радою Вінницького національного технічного університету Міністерства освіти і науки України.

Квєтний Р.Н., Кривогубченко С.Г., Кривогубченко Д.С., Богач І.В.,
К 89 **Прадівлянний М.Г. Інтегральна схемотехніка** / Навчальний посібник.
– Вінниця: ВНТУ, 2005. – 59 с.

Посібник присвячено розгляду арифметичних та логічних основ цифрової техніки, синтезу комбінаторних мереж, реалізації елементів та вузлів цифрової техніки (логічних елементів, тригерів, регістрів, лічильників, перетворювачів кодів, запам'ятовувальних пристроїв, логічних матриць та пристроїв відображення інформації).
Призначений для курсу "Інтегральна схемотехніка".

УДК 621.31

INTRODUCTION

Rapid development of modern microelectronics and digital equipment is connected with the growing number of systems designers. They are interested in modern literature where there is both information about traditional designing of circuit techniques and about the new applications and solutions.

An expert in the field of digital circuitry should:

- have diverse knowledge in methods of mathematical description of operation of digital circuits at logical and electrical levels;
- know modern component basics of digital circuitry;
- understand the industrial series of integrated chips and perspectives of their further improvement;
- master the methods of structural construction of digital devices and systems.

The suggested textbook considers general information about the integrated circuits (classification, system of symbolic notations, types of 1C cases), arithmetical and logical bases of digital engineering, methods of synthesis of combinative circuits, logical elements and triggers. It also describes the examples of application of digital elements in impulse circuits and the rule of circuit engagement of elements. A lot of attention is paid to consideration of units of digital engineering (registers, counters, converters of codes, storage devices, logical arrays and displaying units).

CONTENT

1 GENERAL INFORMATION ABOUT THE INTEGRATED CIRCUITS

1.1 Basic terms and definitions

Modern systems of automation and management use electrical signals [1], for which a large speed of processing, wide range, simplicity of forming, transfer and transformations to other kinds of energy are inherent. During forming, transfer and processing the electrical signals can be subject to different transformations. The electrical systems, which consist of electronic passive electrical elements (resistors, condensers, inductors), are used for this purpose. The performance of electronic systems is determined by the performances of their component electronic elements, which are manufactured in two kinds:

- as separate discrete components (diodes, transistors, thyristors and so forth);
- as chips (integrated circuits).

An integrated chip (IC) is a microelectronic item [2], which performs functions of transformation, processing and accumulation of information and has a high denseness of packing of electronically connected elements and crystals, which are considered as a single whole.

Element of IC is a part of IC, which performs a function of some radio component (for example of transistor, diode, resistor, condenser) and is made inseparable with crystal.

Degree of IC integration is evaluated by a parameter (factor) of a degree of complexity:

$$\mathbf{K=\lg N,} \tag{1.1}$$

where **N** is an amount of elements, that form the IC.

In correspondence with this formula the chips of the first degree of integration contain up to 10 elements and components, the chips of the second degree - up to 100, the chips of the third degree - up to 1000 and so forth.

ICs are developed and produced in the form of series. Each series differs by a degree of completeness and totals several chips.

A series is an aggregate of chip types, each of which performs various functions, but have common structurally technological completion. They are intended for joint use.

Type of IC is a specific functional designing of the chip.

1.2 Classification of IC

Depending on the process of manufacturing IC can be semi-conducting, film-like or hybrid.

Semi-conducting IC is a chip, all elements and inter-element junctions of which are performed within the semiconductor and its surface.

Film-like IC is a chip, all elements and inter-element junctions of which are performed in the kind of conductive films and dielectric elements.

Hybrid IC is a chip, which, besides elements, contains simple and complex components (for example crystals of semi-conducting ICs).

Depending on functional designing of IC they are subdivided into analog and digital.

Analog ICs are intended for transformation and processing of signals, which are changed under the law of continuous function.

The signals, which are changed under the law of discrete function, are transformed and processed with help of **digital ICs**.

Depending on level of the integration ICs are subdivided into: **SIC** (small degree of integration) - up to 100 elements on crystal; **AIC** (average degree of integration) - up to 1000 elements on crystal; **LIC** (large degree of integration) - up to 10000 elements on crystal; **SLIC** (the super-large degree of integration) - more than 10000 elements on crystal.

Creation of complex chips, in the process of development and organization of manufacturing of which the factory-customer takes part together with the factory-producer, is being wide spread now along with the development of the chips of general purpose. Ordered and half-ordered chips belong to IC.

Ordered IC is a chip, which is developed on the basis of standard and (or) specially created elements and units according to the functional scheme of the customer.

Half-ordered IC is a chip, which is developed on the basis of base crystals.

The classification of IC according to the type of to be executed functions is given in table 1.1. The letter designations are given alphabetically.

Table 1.1- **Classification of IC**

Subgroup and kind of IC	**Symbol**
1	2
Formers	
of address currents	АА
of impulses of the rectangular form	АГ
of discharge currents	АР
other	АП
of impulses of the special form	АФ
Delay circuits	

Continuation of table 1.1

passive	БМ
other	БП
active	БР
The circuits of computing devices	
of junction with a bus	ВА
of synchronization	ВБ
of input-output control	ВВ
controllers	ВГ
micro – ECM	ВЕ
specialized	ВЖ
timing	ВИ
combined	ВК
microprocessors	ВМ
of interrupt control	ВН
other	ВП
functional extenders	ВР
microprocessor sections	ВС
of memory control	ВТ
of microprogram control	ВУ
functional converters	ВФ
microcalculators	ВХ
Generators	
of square signals	ГГ
of linear-variable signals	ГЛ
of noise	ГМ
other	ГП
of harmonic signals	ГС
of special form signals	ГФ
Detectors	
amplitude	ДА
impulse	ДИ
other	ДП
frequency	ДС
phase	ДФ
The circuits of blocks of a secondary power supply	
rectifiers	ЕВ
impulse stabilizers of volt	ЕК
converters	ЕМ
stabilizers of continuous voltage	ЕН
other	ЕП
of the power supply	ЕС
stabilizers of a current	ЕТ
impulse voltage stabilizers control	ЕУ

Continuation of table 1.1

The schemes of digital devices	
arithmetic-logic	ИА
encipherers	ИВ
decoders	ИД
counters	ИЕ
combined	ИК
half-adders	ИЛ
adders	ИМ
other	ИП
registers	ИР
Switchboards and keys	
of voltage	КН
other	КП
of current	КТ
Elements of logic	
AND-NOT	ЛА
AND-NOT / OR-NOT	ЛБ
extenders	ЛД
OR-NOT	ЛЕ
AND	ЛИ
AND-OR-NOT / AND-OR	ЛК
OR	ЛЛ
OR-NOT / OR	ЛМ
NOT	ДН
other	ЛП
AND-OR-NOT	ЛР
AND-OR	ЛС
Modulators	
amplitude	МА
impulse	МИ
other	МП
frequency	МС
phase	МФ
Set of elements	
of diodes	НД
of condensers	НЕ
combined	НК
other	НП
of resistors	НР
of transistors	НТ
functional	НФ
Converters	
digital – analog	ПА

Continuation of table 1.1

analog – digital	ПВ
of duration	ПД
multipliers of analog frequency	ПЕ
deviders of analog frequency	ПК
synthesizers of frequency	ПЛ
of power	ПМ
of voltage (current)	ПН
other	ПП
code – code	ПР
of frequency	ПС
of level	ПУ
digital deviders of frequency	ПЦ
The circuits of storage devices	
associative	РА
matrixes of constants SD	РВ
ROM (mask)	РЕ
matrixes of on-line memory	РМ
other	РП
reprogrammable ROM	РР
one-time programming ROM	РТ
RAM	РУ
ROM with ultra-violet erasing	РФ
SD on cylindrical magnetic domains	РЦ
The comparison circuits	
amplitude	СК
by voltage	СА
by time	СВ
other	СП
frequency	СС
Triggers	
of JK type (universal)	ТВ
dynamic	ТД
combined	ТАК ЯК
of Shmidt	ТЛ
of type D	ТМ
other	ТП
of type RS	ТР
of type T (counting)	ТТ
Amplifiers	
of high frequency	УВ
operational	УД
repeaters	УЕ
of impulse signals	УИ

Continuation of table 1.1

wideband	УК
of reading and restoring	УЛ
of indication	УМ
of low frequency	УН
Other	УП
of intermediate frequency	УР
differential	УС
of direct current	УТ
Filters	
of the upper frequencies	ФВ
band	ФЕ
of the lower frequencies	ФН
other	ФП
rejector	ФР
The multifunctional circuits	
analog	ХА
combined	ХК
digital	ХЛ
digital matrixes	ХМ
analogue matrixes	ЗН
combined matrixes	ХП
The photosensing circuits with charge connection	
linear	ЦЛ
matrix	ЦМ
other	ЦП

1.3 System of IC conventional symbols

Information about the functionality and design of a chip is located in its conventional symbols. According to the normative documents labels of integrated chips consist of 4 elements:

The First is a digit that indicates structurally technological fulfillment.

1,5,6,7 (bare chip) - semiconducting IC; 2,4,8 - hybrid;

3 - other (R, C sets, of special assemblage).

The Second - two-three digits, which specify a serial number. First two elements designate number of a IC series.

The Third - two letters, which designate a subgroup and kind of a chip (table 1.1)

The Fourth - serial number of IC according to the functional indication in the given series. The letters K, M, P, Ф, E placed before a symbolic notation of a chip characterize the conditions of their monitoring at the enterprise and features of design fulfillment (K - wide consumption, if K is absent - special purpose - increased reliability; M - ceramic case, P - plastic, Ф - miniature, E - export fulfillment). The letter that indicates a dispersal of electrical parameters of chips is sometimes put at the end of the symbolic notation.

An example of symbolic notation of IC:

	I	II	III	IV		
	1	33	ЛА	3		Four logic elements 2 AND-NOT of spec. purpose
K	1	108	ПА	1		DAC of wide use
KP	1	40	УД	1		RAM of wide use in plastic case
KP	5	80	BM	80	A	CPU of wide use in plastic case

In conventional symbols of IC, produced in an open-case design, the letter B is placed before the series number.

1.4 Typical cases of IC

IC case is intended to protect it from external influences and to ensure its normal work within the whole period of its operation. Five types of structural technological fulfillment of IC are most widely spread. The design of rectangular case with outlets, that are perpendicular to the plane of the basis and located within the limits of a projection of a case body on a plane of the basis, is schematically shown in figure 1.1.

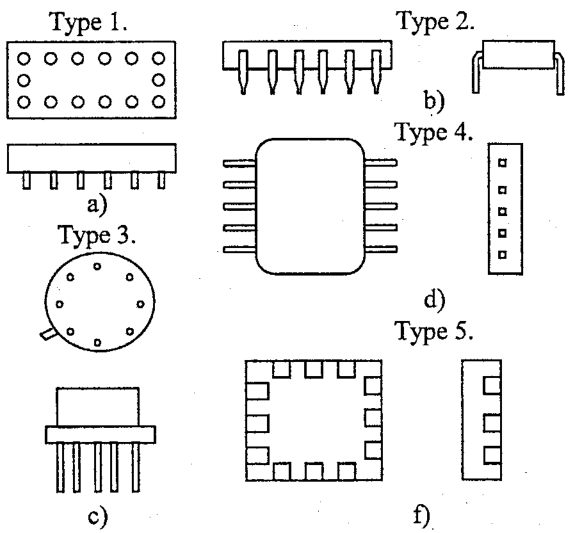


Figure 1.1 - Types of cases

Case of the second type (the type ДИП) - with rectangular conclusions, which are perpendicular to the plane of the case basis, that exceed the bounds of projection of a case skew field on the plane of the basis, is shown in figure 1.1, b and a round case with outlets, which are perpendicular to the case basis and located within the limits of a projection of a case skew field on the plane of the basis (case of the third type), - in figure 1.1, c. The rectangular case with outlet located parallel to the plane of the basis, which exceed the bounds' projections of its skew field on the plane of the basis (case of the fourth type), is shown in a figure 1.1, d.

The case of the fifth type, rectangular, flat, «leadless», with metal platforms on a perimeter of case is shown in figure 1.1, f.

2 DIGITAL IC

2.1 Arithmetical fundamentals of digital engineering

2.1.1 Numerical systems

In discrete engineering all information, regardless of its type, is presented in numerical way [3], and only the positional systems of calculation are used. In these systems any number A can be represented as:

$$A = \sum_{i=-m}^{n-1} a_i h^i , \tag{2.1}$$

Where: a_i - digits;

h^i - basis of a system;

n - number of signs before a comma;

m - number of signs after a comma.

Depending on a basis, the positional notation can be decimal - with a basis 10, binary - with a basis 2 etc. The usual decimal system uses figures 0,1,2....., 9, thus, for example, number 25.5 can be presented as

$$(25.5)_{10} = \underbrace{2 \cdot \overbrace{10^1 + 5 \cdot 10^0 + 5 \cdot 10^{-1}}^{h_i}}_{a_i}$$

A binary numerical notation, for which two digits 0 and 1 are enough, is most widely spread in the field of computer techniques. The binary place represents the least amount of information, which is named as bit.

The octal and hexadecimal systems are used more often among other numerical calculus. In an octal system digits are represented by the same symbols, as in decimal, and in hexadecimal system six symbols A, B, C, D, E, F are added. They correspond to decimal numbers 10,11,12,13,14,15. The notations of the first 32 numbers in numerical systems 2,8,16 are shown in table 2.1.

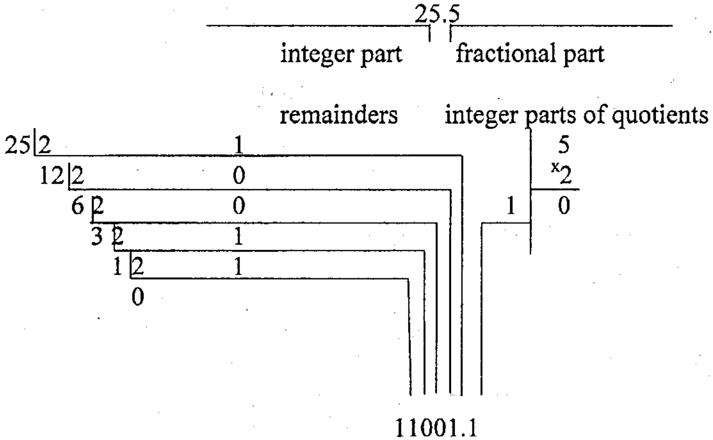
Table 2.1 - **Representation of numbers in various numerical notations**

Decimal number	**In num. notation with base**			**Decimal number**	**In num. notation with base**		
	2	**8**			**2**	**8**	**16**
0	0	0	0	16	10000	20	10
1	1	1	1	17	10001	21	11
2	10	2	2	18	10010	22	12
3	11	3	3	19	10011	23	13
4	100	4	4	20	10100	24	14
5	101	5	5	21	10101	25	15
6	110	6	6	22	10110	26	16
7	111	7	7	23	10111	27	17
8	1000	10	8	24	11000	30	18
9	1001	11	9	25	11001	31	19
10	1010	12	A	26	11010	32	1A
11	1011	13	B	27	11011	33	1B
12	1100	14	C	28	11100	34	1C
13	1101	15	D	29	11101	35	1D
14	1110	16	E	30	11110	36	1E
15	1111	17	F	31	11111	37	1F

The greatest decimal number, which is possible to represent by n-digit number in a numerical notation with a basis h, equals to (h^n-1). To represent h^n it is necessary to have h of different digits for every stage, that is g = n*h of digits. At the same time amount of numbers, which can be presented in a system with the basis h, placing g digits, is determined by function $h^{g/h}$. It reaches the maximum under condition of equality of h with a basis of hyperbolic logarithms e ≈ 2.7, which specifies a ternary system as the most economic. In due course this conclusion has become one of the basic for construction of ternary computers, but the development of integrated technology has reduced its influence. Since then the binary numerical notation has taken the dominant significance in computer techniques.

2.1.2 Transformation of numbers

Common task in digital engineering is a process of changing the decimal numbers to binary and back. It can be done with the help of universal algorithm, which is used separately for the integer and fractional parts. Changing of the integer part of a decimal number to a binary system lies in the recording of residuals (0 or 1) in the reversed order, which are received during division of an initial number and each following divider by two. The fractional part is got from the integer parts (0 or 1) with its sequential multiplication by two. Such multiplication lasts until the fractional part turns to zero or the necessary amount of symbols after digital point is received. It is illustrated in the following example.



Using expression (2.1), it is possible to represent an outcome of transformation as

$(11001.1)_2 = 1*2^4 + 1*2^3 + 0*2^2 + 0*2^1 + 1*2^0 + 1*2^{-1} = 16 + 8 + 1 + 0.5 =$ 25.5

To change the octal and hexadecimal numbers to binary numbers, it is sufficient to represent each position by three binary positions (triad) for the octal numbers, and by four binary positions (quaternion) for hexadecimal numbers. For example:

$$(31.4)_8 = (011001.100)_2$$
$$(19.8)_{16} =(00011001.1000)_2$$

The reverse change of binary number to octal or hexadecimal is executed by its division on blocks (triads or quaternions) to the left and to the right from a dividing symbol. The insufficient positions in extreme left and right blocks are supplemented by zeroes. Then each triad is substituted by an octal, and each quaternion - by a hexadecimal number. The octal and hexadecimal representation of binary numbers is used for the most compact notation. Hexadecimal form is more convenient for the representation of the larger unit of information - byte that is equal to eight bits, for what the two-place hexadecimal number suffices.

For the transformation of a number from any numerical notation to decimal it is enough to calculate the value of an appropriate polynomial, by substituting to it the decimal values of the positions and bases of a numerical notation. The calculation is convenient for executing by Horner's method, which is based on representation of a polynomial (2.1) as

$$(...((a_{n-1} \cdot h + a_{n-2}) \cdot h + a_{n-3}) \cdot h + ... + a_1) \cdot h + a_0,$$

that is the digit a_{n-1} of a top position of number, which is being changed, is multiplied on a basis of h of an initial numerical notation and the outcome is added to the following digit, then the process is repeated up to the smallest digit position. For example:

$$(5327)_8 \quad 5 * 8 + 3 \Rightarrow 43 * 8 + 2 \Rightarrow 346 * 8 + 7 = (2775)_{10}$$

2.1.3 Inverted and zero-complement codes

The inverted code of n-digit number A with the basis h supplements it up to the greatest possible value h^n-1, that is $A_0 = h^n-1-A$. And the digit of each position of an inverted code A_0 supplements an appropriate digit of the beginning number A up to the greatest digit h-1 (for a decimal number - up to 9). The zero-complement code of number A is received as a residual $A_0 = h^n - A$, that is, it is larger than an inverted code by 1.

The sum of the integer binary numbers with allowance of signs can be reduced to the sum of their zero-complement or inverted codes. An inverted code for a negative number is received by a direct replacement of 0 to 1 and 1 to 0 in all positions. To represent the number in the zero-complement code, it is enough to add 1 to an inverted code.

The sum in zero-complement code is received by the rules of binary arithmetic – position by position, taking the sign digits into account. Carry from a sign digit is possible. For example:

$(+9)_{10} = 0\ 1001$ ______________ 01001

$^{+}(-5)_{10} = \underline{1\ 0101} \Rightarrow 1010$

$+\underline{\quad 1}$

zero-complement code 1011 ______________ $\underline{11011}$

1,00100

The carry is ignored

An inverted code may be used for the algebraic sum. For example:

$$\begin{array}{lr}
(+9)_{10} = 0\ 1001 & \underline{\qquad\qquad 01001} \\
(-5)_{10} = 1\ \underline{0101} \Rightarrow 1\ 1010 & \underline{11010} \\
 & 1\ 00011 \\
\text{inverted code} & \underline{\hookrightarrow +1} \\
 & 00100
\end{array}$$

The subtraction in zero-complement and inverted codes is carried out by adding by a method of a replacement of a sign (and code) of the subtrahend.

2.1.4 Binary decimal codes

Binary decimal coding is used in the digital devices for the representation of an information in a decimal numerical notation and for execution of operations on decimal numbers. Binary decimal coding represents each decimal digit by group of binary digits. The amount of bits in such a group is precisely fixed (there should be not less than four of them) with preservation of all left-hand zero positions. There are several types of binary decimal codes (table 2.2).

Table 2.2 - **Types of binary decimal codes**

Decimal digits	**Binary codes of decimal digits**			
	8421	**2421**	**with remainder 3**	**2 of 5**
0	0000	0000	0011	11000
1	0001	0001	0100	00011
2	0010	0010	0101	00101
3	0011	0011	0110	00110
4	0100	0100	0111	01001
5	0101	1011	1000	01010
6	0110	1100	1001	01100
7	0111	1101	1010	10001
8	1000	1110	1011	10010
9	1001	1111	1100	10100

The code of direct substitution is considered to be the most widespread and used. In this code an appropriate four-digit binary number substitutes each digit of the decimal number. Its other name - code 8421 - reflects the significance of weight factors, which are attributed to appropriate bits in a group. In accordance with this it is also named weighted code. Convenience of this code becomes apparent during the transformation from a decimal system to binary and back, and also during addition in usual binary summators, because of its additivity (the sum of codes of two digits represents a code of the sum).

Residual of a quaternion, that allows 16-code combinations, allows creating other variants of binary decimal codes. Code 2421 is one of them. Its feature is that the replacement in a coding quaternion of zeroes to ones, and ones to zeroes, converts each decimal digit A to 9-A, that is the inverted code is received. For its transformation into zero-complement code it is enough to add 1. The codes with such properties are called self-adding. They are used during the fulfillment of arithmetical operations on decimal numbers in the inverted and zero-complement codes.

Self-adding is also a code with excess 3, which is received by adding $3_{10} = 0011_2$ to each digit of a code of direct substitution. As well as code 2421, it is convenient for fulfillment of operations on decimal numbers. And the carries are easily determined, as the sum of two additions, each of which is taken with excess 3, is received with excess 6, that excludes superfluous code combinations (3 is subtracted from an outcome for receiving the correct code of the sum). But this code, as opposed to codes 8421 and 2421, is not weighted, therefore is not convenient for transformation of numbers from one notation to other. The binary decimal codes, in which coding quaternions are supplemented by redundant bits to use this redundancy for supplementing these codes with the specific properties, which are needed for error detection and by that for increasing the reliability of computing systems, are also used.

So in code 2 each decimal digit from 5 is given in 5 digit positions, and only 2 of them comprise unities that allows to defect single errors.

The operations on decimal digits are executed with the help of supplemented binary arithmetic. Thus, when adding two numbers in a code of direct substitution 8421 it is necessary to add the correcting element $6_{10} = 0110_2$ to each quaternion, in which during addition figure > 9 is obtained or there was a carry in the following quaternion. For example:

$$\begin{array}{rr}
38_{10} = & 0011\ 1000 \\
\underline{+16_{10} =} & \underline{0001\ 0110} \\
 & 0100\ 1110 \\
\text{Correction} & \underline{+0000\ 0110} \\
54_{10} = & 0101\ 0100
\end{array}
\qquad
\begin{array}{rr}
29_{10} = & 0010\ 1001 \\
\underline{+58_{10} =} & \underline{0101\ 1000} \\
 & 1000\ 0001 \\
\text{Correction} & \underline{+0000\ 0110} \\
87_{10} = & 1000\ 0111
\end{array}$$

During the subtraction of numbers in a code 8421 the correction comes to subtraction $6_{10} = 0110_2$ from each quaternion of difference, which needs borrowing.

For example:

$$\begin{array}{rr}
63_{10} = & 0110\ 0011 \\
\underline{-27_{10} =} & \underline{0010\ 0111} \\
 & 0011\ 1100 \\
\text{Correction} & \underline{-0000\ 0110} \\
36_{10} = & 0011\ 0110
\end{array}$$

2.1.5 Gray code

Among the binary codes, that were not weighted, where the transition towards adjacent is accompanied by modifications only in one position (Codes with exchanged unity) – Gray code (table 2.3), are of special use.

Table 2.3 - **Gray Code**

Decimal numbers	Binary code	Gray Code
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0101
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

The transition from a binary code towards a Gray code and back is made according to the rule (figure 2.1, a): the high-order bits coincide, and any following bit of a Gray code equals to the sum modulo 2 (⊕) of the appropriate and previous bits of a binary code (disregarding of transposition in a high-order bit). During the reverse transition (figure 2.1, b) high-order bits also coincide, but each following bit is received as the result of adding modulo 2 of the obtained previous bit of a binary code and an appropriate bit of a Gray code.

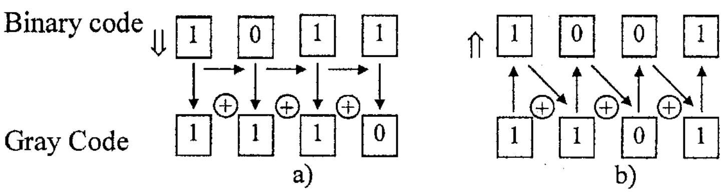


Figure 2.1 - Transformations to a Gray code and back

2.1.6 Alphanumeric codes

For the representation of alphanumeric information in the computing system it is necessary to encode all symbols - digits, letters, mathematical and special signs, command characters and other, which form its alphabet. The most frequently used standard among them is ASCII (American Standard Code for Information Interchange), which is put in a basis of state standard KOI - 7 [4]. In table 2.4, a 7-bit code for information interchange and processing (KOI-7) is shown in decimal, octal and hexadecimal numerical notations. The standard code contains:

a) graphical symbols (columns from 3 on 8), which include the Latin letters, Arabic numbers, signs of arithmetical and logical operations, separating signs and others;

b) control symbols (columns 1 and 2), which are used for controlling of data transfer equipment, for controlling of input-output devices, and also for division of an information by parts in correspondence with its logical structure.

A hexadecimal number that corresponds to the first symbol in this column identifies each column of the table. The code of any symbol in the table is determined by a hexadecimal number, which is received by adding of number of a column to number of line. For example, the letter «K» is in column «40» and line «B», therefore its hexadecimal code equals to 4B.

The code of a symbol in other numerical notations is shown to the left of each symbol: above - in decimal, below – in octal. So the symbol «K» has a code 75 in a decimal system and 133 - in octal.

Table 2.4 - **KOI - 7**

Number	**Control symb.**				**Graphic symbols**											
	00		**10**		**20**		**30**		**40**		**50**		**60**		**70**	
1	2		3		4		5		6		7		8		9	
0	0	ПУС	16	АР1	32	_	48	0	64	@	80	P	96	‘	112	p
	0		20		40		60		100		120		140		160	
1	1	НЗ	17	СУ1	33	!	49	1	65	A	81	Q	97	a	113	q
	1		21		41		61		101		121		141		161	
2	2	НТ	18	СУ2	34	“	50	2	66	B	82	R	98	b	114	r
	2		22		42		62		102		122		142		162	
3	3	КТ	19	СУ3	35	#	51	3	67	C	83	S	99	c	115	s
	3		23		43		63		103		123		143		163	
4	4	КП	20	СУ4	36	$	52	4	68	D	84	T	100	d	116	t
	4		24		44		64		104		124		144		164	
5	5	КТМ	21	НЕТ	37	%	53	5	69	E	85	U	101	e	117	u
	5		25		45		65		105		125		145		165	

Continuation of table 2.4

1	2		3		4		5		6		7		8		9	
6	6 6	ДА	22 26	СИН	38 46	&	54 66	6	70 106	F	86 126	V	102 146	f	118 166	v
7	7 7	ЗВ	23 27	КБ	39 47	‘	55 67	7	71 107	G	87 127	W	103 147	g	119 167	w
8	8 10	ВШ	24 30	АН	40 50	(	56 70	8	72 110	H	88 130	X	104 150	h	120 170	x
9	9 11	ГТ	25 31	КН	41 51	)	57 71	9	73 111	I	89 131	Y	105 151	i	121 171	y
A	10 12	ПС	26 32	ЗМ	42 52	*	58 72	:	74 112	J	90 132	Z	106 152	j	122 172	z
B	11 13	ВТ	27 33	АР2	43 53	+	59 73	;	75 113	K	91 133	[	107 153	k	123 173	{
C	12 14	ПФ	28 34	РФ	44 54	,	60 74	<	76 114	L	92 134	\	108 154	l	124 174	|
D	13 15	ВК	29 35	РГ	45 55	-	61 75	=	77 115	M	93 135	]	109 155	m	125 175	}
E	14 16	ВИХ	30 36	РЗ	46 56	.	62 76	>	78 116	N	94 136	^	110 156	n	126 176	~
F	15 17	ВХ	31 37	РЕ	47 57	?	63 77	?	79 117	O	95 137	_	111 157	o	127 178	ЗБ

2.2 Logical fundamentals of digital engineering

2.2.1 Main provision of algebra of logic

The analysis and synthesis of logic circuits is made with the help of mathematical means of algebra of logic or Boolean algebra [3,5,6,7], in which variables can acquire only one of two values: 0 or 1. Three main operations can be executed over variables: the logical addition, logical multiplication and logical negation, that corresponds to logical functions OR, AND, NOT.

The logical adding (alternation) is designated by a symbol "+" or V (first letter of a Latin word vel - or). As an example of a circuit, which realizes a function OR, it is possible to cite a parallel junction of closing contacts of several relays (figure 2.2, a). The circuit, which includes these contacts, will be closed, if at least one relay is activated.

Thus, the logic sum is equal to one, when one or several addends are equal to one:

$$0+0=0; \qquad 0+1=1; \qquad 1+0=1; \qquad 1+1+....+1=1$$

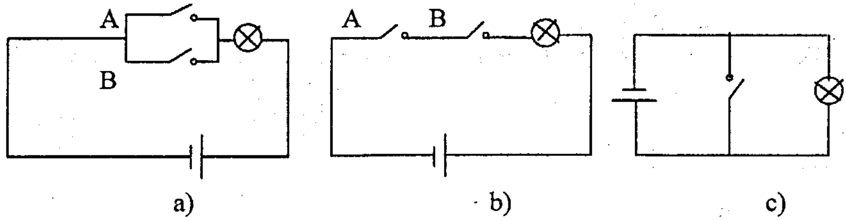


Figure 2.2 - Electrical realization of general logical functions

The function of transformation is most visually characterized by the table, in which each combination of source variables X corresponds to the value of target variable Y. It is called a truth table (table 2.5).

Table 2.5- **General logical functions**

X1	**X2**	**АБО OR**	**І AND**	**НІ NOT**
		$Y = X1+X2$	**$Y = X1*X2$**	**$Y = \overline{X1}$**
0	0	0	0	1
0	1	1	0	1
1	0	1	0	0
1	1	1	1	0

A point designates the logical multiplication (conjunction). In Boolean formulas it is not designated in any way. The function OR is realized, for example, by sequentially joint closing contacts of several relays (figure 2.2, b). The circuit in this case will be closed only when all relays will work:

$$0*0=0; \qquad 0*1=0; \qquad 1*0=0; \qquad 1*1=1.$$

A line above a label of argument designates the logical negation (inversion). By a model, which realizes a function NOT, there can be a circuit in a figure 2.2, or breaking contact relay. The circuit, which includes such contact, is broken during an operation of the relay. Thus, the inversion of one is equal to zero, and the double inversion does not change the variable:

$$\overline{0} = 1; \qquad \overline{1} = 0; \qquad \overline{\overline{0}} = 0; \qquad \overline{\overline{1}} = 1$$

Any complicated functions; given in table 2.6, can be expressed by conjunction, disjunction and inversion.

The above allows to note the following:

$$a+0=a; \qquad a+1=1; \qquad a+a+.....+a=a; \qquad a+\overline{a}=1$$
$$a*0=0; \qquad a*1=a; \qquad a*a*.....*a=a; \qquad a*\overline{a}=0; \qquad a=\overline{\overline{a}}$$

Table 2.6- **Logical functions**

X1	X2	Sheffer's Function	Function of the Peirce	Sum modulo 2
		$Y = \overline{X1 * X2}$	$Y = \overline{X1 + X2}$	$Y = X1 \oplus X2$
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	0	0	0

2.2.2 General laws of algebra of logic

Law of transition:

$$a + b = b + a$$

Law of junction:

$$(a + b) + c = a + (b + c); \quad (a * b) * c = a * (b * c)$$

Law of distribution:

$$a * (b + c) = a * b + a * c; \qquad a + b * c = (a + b)(a + c)$$

Law of absorption:

$$a + a * b = a(1 + b) = a; \qquad a(a + b) = a + a * b = a$$

Law of a pasting together:

$$a * b + a * \bar{b} = a; \qquad (a + b)(a + \bar{b}) = a$$

Law of negation:

$$\overline{a + b} = \bar{a} * \bar{b}; \qquad \overline{a * b} = \bar{a} + \bar{b}$$

$$\overline{\bar{a} + \bar{b}} = a * b; \qquad \overline{\bar{a} * \bar{b}} = a + b$$

The law of negation (it is often named as the rule of de Morgan) is applicable for any number of variables.

$$\overline{a + b + \ldots + z} = \bar{a} * \bar{b} * \ldots * \bar{z};$$

$$\overline{a * b * \ldots * z} = \bar{a} + \bar{b} + \ldots + \bar{z};$$

2.2.3 Functional completeness

The system of functions, by the superposition of which any function can be represented, is named as **functional completeness**. The combination of simplest functions – conjunction, disjunction and inversion, is functionally complete. For example: the function $a*\bar{b} + \bar{a}*b$ can be represented by two elements NOT (they are necessary to receive inversions of a and b), two elements AND, which are necessary to receive logic multiplication $a*\bar{b}$ and $\bar{a}*b$, and element OR, that will add obtained values.

The functionally full circuits can consist of a group of elements, which realize logical functions that are distinct from elementary. Functionally complete circuits can be made from elements of only one type, for example, of realizing function AND-NOT or OR-NOT. Let's look at the possibility of construction of logical circuits, which realizes the elementary functions on the basis of element AND-NOT. Function NOT, that is the inversion of variable, is possible to realize, if the signal, which corresponds to this variable, is given on one of inputs of a circuit AND-NOT, and a steady signal, which corresponds to one, is given on the other inputs: $\overline{a*1*......*1} = a$. For the creation of a circuit AND it is enough to include sequentially circuit AND-NOT and inverter: $\overline{\overline{a*b}} = a*b$. The circuit OR is created in the correspondences with the rule of de Morgan: $\overline{\bar{a}*\bar{b}} = a+b$. Thus circuits AND-NOT allow to realize inversion, conjunction and disjunction, and accordingly on their basis it is possible to construct circuits for realization of any composite functions.

The element OR-NOT also allows to realize the elementary functions. To receive the inversion of one variable it is enough to give a signal, appropriate to this variable, on one input of a circuit OR-NOT, and on other inputs - levels of logic zero. The function OR can be realized by inverting a target signal of a circuit OR-NOT. The function AND will be realized with the help of elements OR-NOT on the basis of law of negation $\overline{\bar{a}+\bar{b}} = ab$.

The possibility of realization of the elementary logic functions testifies to the functional completeness of logic elements AND-NOT and OR-NOT.

2.2.4 Standard forms

Any logical function $F(X_1, ..., X_n)$ can be presented in perfect disjunctive normal form (PDNF):

$$F(X_1, ..., X_n) = \bigvee_{i=0}^{N-1} C_i^{1}*F(A_i) =$$

$$=C_0^{1}*F(A_0) \vee C_1^{1}*F(A_1) \vee ...... \vee C_{N-1}^{1}*F(A_{N-1}) \qquad (2.2)$$

or in perfect conjunctive normal form (PCNF):

$$F(X_1, ..., X_n) = \bigwedge_{i=0}^{N-1} [C_i^{0} \vee F(A_i)] =$$

$$=[C_0^{0} \vee F(A_0)]\cdot[C_1^{0} \vee F(A_1)]......[C_{N-1}^{0} \vee F(A_{N-1})], \qquad (2.3)$$

where F (A_i) - value of function (0 or 1), which it accepts on a set A_i;

$C_i^1 = X_1 * X_2 * \ldots\ldots * X_N$ – Minterm;

$C_i^0 = X_1 V X_2 V \ldots\ldots V X_N$ – Maxterm.

We shall illustrate the representation of logical function according to the specific table of correspondence (table 2.7)

Table 2.7 - **The table of correspondence**

A_I			$F(A_i)$
X_1	X_2	X_3	X_4
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

For the representation of logical function in PDNF it is enough to use only those sets of variables Ai, on which $F(A_i)=1$, because when $F(A_i)=0$, conjunction $C_i^1 * F(A_i)=0$. For the representation in PCNF those sets of variables Ai are used, on which F $(A_i)=0$, because when F $(A_i)=1$ disjunction $[C_i^0 V F(A_i)]=1$, regardless of value of C_i^0. This is why the PDNF is called a form of representation by ones, and PCNF is called a form of representation by zeroes.

PDNF $\quad Y = \overline{X_1}\,\overline{X_2}\,X_3 + \overline{X_1}\,X_2\overline{X_3} + \overline{X_1}\,X_2X_3 + X_1\overline{X_2}\,\overline{X_3} + X_1X_2\overline{X_3} + X_1X_2X_3$

PCNF $\quad Y = (X_1+X_2+X_3)*(X_1+\overline{X_2}+\overline{X_3})*(\overline{X_1}+\overline{X_2}+X_3)$

2.2.5 Synthesis of combinative circuits

The combinative logical circuits are such circuits, target signals of which do not depend on prehistory and are unambiguously determined by signals present on their inputs in the given instant. In other words combinative circuits are the circuits, in which there are no elements of memory.

The synthesis of combinative circuits is carried out in the following sequence. The table of operation of a logic circuit - truth table - is made at first, proceeding from which the logical function is noted, then the minimization and transformation to a kind convenient to realization on logic elements of a specific type is carried out.

Let's consider in details the process of synthesis of combinative circuits on an example. Lets assume that it is necessary to construct a majoritary element (element of a voting) with three inputs, that is such an element, which signal on an output is equal to one, when the majority of source signals is equal to one. Let's make the truth table (table 2.8).

Table 2.8 - **Truth table**

N	X_1	X_2	X_3	**F**
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	1
4	1	0	0	0
5	1	0	1	1
6	1	1	0	1
7	1	1	1	1

$$F = \overline{X_1}X_2X_3 + X_1\overline{X_2}X_3 + X_1X_2\overline{X_3} + X_1X_2X_3 \qquad (2.4)$$

Using the table 2.8, we shall note logic function. To do this we shall present it as the sum of logic addends (PDNF), which correspond to those lines of table 2.8, for which the function F equals to one:

For minimization of function (2.4) we use the main laws of algebra of logic:

$$\begin{aligned} F &= \overline{X_1}X_2X_3 + X_1\overline{X_2}X_3 + X_1X_2\overline{X_3} + X_1X_2X_3 = \\ &= (\overline{X_1}X_2X_3 + X_1X_2X_3) + (X_1X_2X_3 + X_1X_2X_3) + \\ &+ (X_1X_2\overline{X_3} + X_1X_2X_3) = X_2X_3 + (\overline{X_1} + X_1) + \\ &+ X_1X_3 + (\overline{X_2} + X_2) + X_1X_2 + (\overline{X_3} + X_3) = \\ &= X_2X_3 + X_1X_3 + X_1X_2. \end{aligned}$$

If elements AND-NOT are used for construction of a logic circuit, it is necessary to transform function to a kind of:

$$F = \overline{\overline{X_1X_2} * \overline{X_1X_3} * \overline{X_2X_3}}$$

As we see, the obtained final expression is obviously easier than the initial.

2.2.6 Minimization with the help of diagrams of Veitch (or maps of Carnot)

In the given example for minimization of a function we used algebraic transformations. This is the universal way, but the final result depends on qualification of the expert, who carries out the minimization. For functions, which have no more than five or six arguments, it is convenient to conduct minimization with the help of diagrams of **Veitch**. This way of minimization guarantees the simplest final expression during the fulfillment of a small amount of the formal rules.

First, it is necessary to present the function in PDNF, to fill in the rectangular table, putting 1 in sections of the table when7an appropriate conjunctions of initial function equals to one, and 0 in remaining sections of the table.

In the filled table all ones are encircled by outlines, and then the minimized function is to be noted as the sum of logic addends, which describe these functions. In the middle of an outline there should be only sections which have been filled in with ones, the number of which should be the integer power of number 2, and the same sections belong to several outlines.

We minimize the function of three variables (2.4) with the help of maps of Carnot (table 2.9).

Table 2.9 - **Minimization of function**

	$\overline{X_2}\,\overline{X_3}$	$X_2\overline{X_3}$	X_2X_3	$\overline{X_2}X_3$
$\overline{X_1}$			1	
X_1		1	1	1

In this case all ones in table 2.9 can be enveloped by three outlines. By noting the labels of these outlines, we shall receive the minimized function

$$F = X_1X_2 + X_1X_3 + X_2X_3$$

2.3 Elements of digital engineering

2.3.1 The basics of digital IC

By digital electronics we mean such schemes, where for each point it is possible to define, as a rule, two states: 0 and 1. For example: 1 - closed contact,

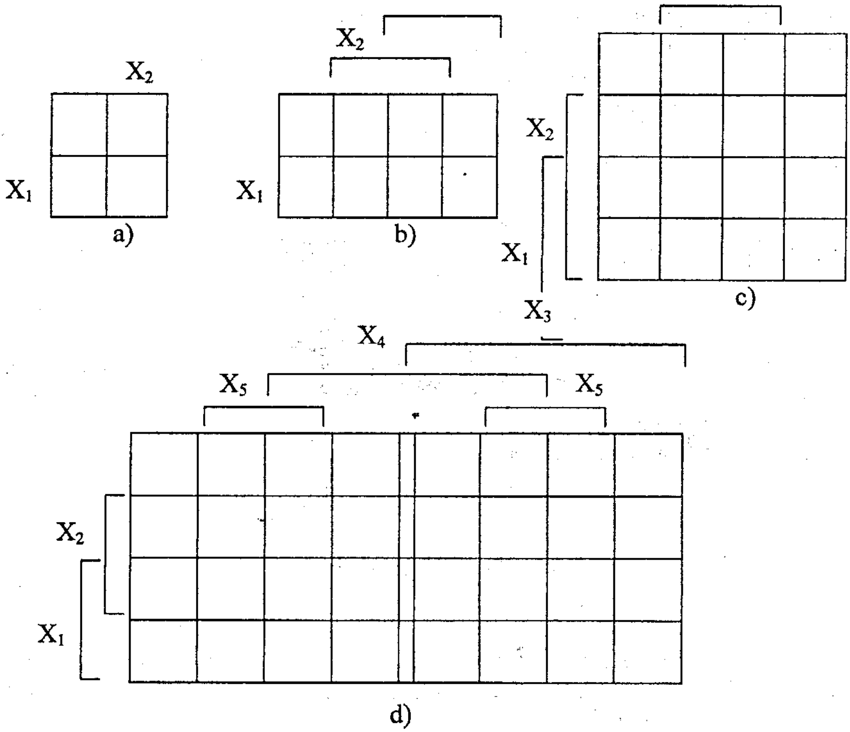


Figure 2.3 - Carnot Maps for a) - two, b) - three, c) - four, d) - five changeable

0 - broken contact; 1 - high level; 0 - low level. The voltage is chosen to be the parameter, precise significance of which does not play a role in digital electronics. The problem lies in recognizing only the equal voltages (figure 2.4)

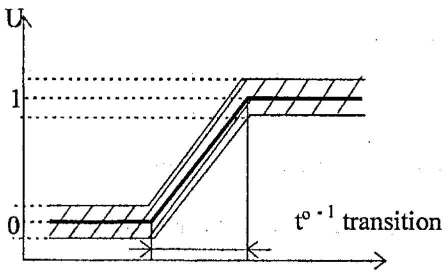


Figure 2.4 - Zones of display of levels of signals

In connection with this for each set of digital-chips the allowable values of high and low levels of voltage are determined. Figure 2.5 shows the values of logic levels for three widespread sets of digital elements.

- TTL - transistor-transistor logic;
- EBL- emitter-bound logic;
- CMDS- logic on complimentary transistors with a metal-dielectric-semiconductor structure.

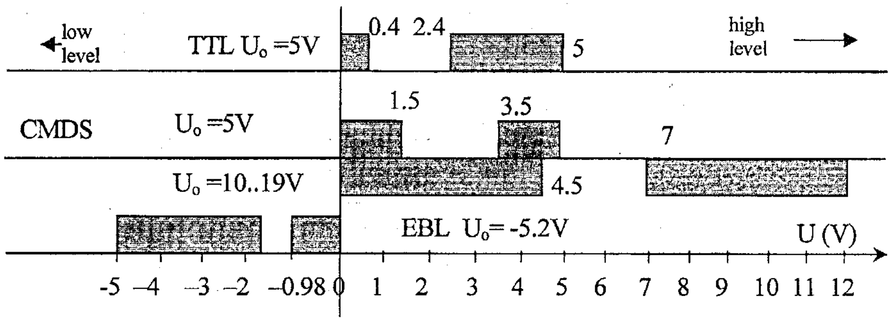


Figure 2.5 - Values of logical levels of digital ICs

Such broad ranges are selected to allow the chips' manufacturer a certain tolerance, within the limits of which the parameters of the scheme can deviate because of a change of temperature, load, power supply voltage and also under the influence of a noise.

Today it is possible to meet different variants of TTL chips in the equipment, which first sets (series K134, K155) are widely substituted by TTLS chips, which have in an internal structure transitions with a Schottky barrier junction (series K531, K555). The use of new integrated transistors with a structure, which is named **«Izoplanar-11»** with oxidizing (instead of p-n by transitions) isolation between adjacent transistors, has allowed to proceed to perspective IC (KP 1531, KP 1533).

The most widespread series of CMDS IC are: K 176, K 561, 564, KP 1561; E3Л IC K 500, 700, K 1500.

The converters (translators) of levels of logic signals are used during the docking of digital instruments constructed on chips of a various type.

2.3.2 General parameters of digital IC

The levels of source and target currents and voltages, values of a potency of consumption, average delay of a signal, which determines the speed of the scheme, output capability, resistance to a counteraction, reliability and other [8], belong to general parameters. Quantitatively load capacity is evaluated by a coefficient of divergence on an output that is by an amount of single loads, which are possible to connect synchronously to an output of a chip. The single load is considered an input of a main logical element of the given series. However, during the increase of an output capability other parameters of IC are worsened, for example the potency of consumption is increased, that's why in the structure of the various schemes there are elements with an increased output capability, thus the output capability is several times larger, than that of the basic elements. The parameter, which is named as energy of switching, is also used for digital chips characterizing.

$$An = P \cdot t_a \tag{2.5}$$

where P - an average power of consumption;
t_a - average delay in signal distribution.

Table 2.10 shows the typical values of parameters of elements of various series are represented. The comparative analysis shows, that the highest speed have the elements EBL and TTLS, that allows them to work with clock frequency -10-100 MHz (EBL) and 5-10 MHz (TTLS). The elements CMDS have a minimum power of consumption - 0.003-0.02 mWt/el. These elements have the lowest energy of switching.

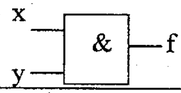
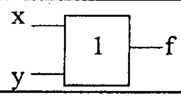
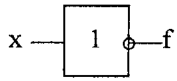
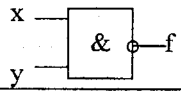
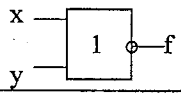
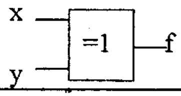
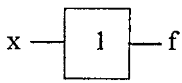
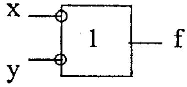
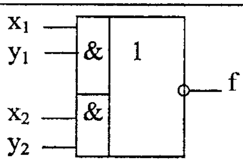
Table 2.10 - **Typical values of parameters of elements of various series**

Parameters		**Typical values of parameters of elements**			
		TTL	**TTLS**	**EBL**	**CMDS**
1		**2**	**3**	**4**	**5**
Levels of source Currents	$I^0_{вх}$, мА	-1.6	-2.0	0.5 мкА	-0.1 мкА
	$I^1_{вх}$, мА	0.04	0.05	0.3	0.1 мкА
Levels of target Voltages	$U^0_{вих}$, В	≤ 0.4	≤ 0.5	≤ -1.6	≤ 1.5
	$U^1_{вих}$, В	≥ 2.4	≥ 2.7	≥ -0.98	≥ 3.5
Power supply voltage	$U_{ж.}$, В	5.0 ± 10%	5.0 ± 10%	-5.2 ± 10%	5...15 ± 10%
Potency of consumption	P, мВт	1 ... 10	2 ... 20	25 ... 40	0.003... 0.02
Delay time	$\tau_з$, нс	30 – 10	10 ÷ 3	2 – 0.75	200 – 50
Energy of switching	$A_п$, пДж	30 – 100	20 – 60	50 – 30	0.6 – 1
Coefficient of branching on an output	$K_{роз.}$	10	8	1	≤ 100

2.3.3 Logical elements

The logical element is an electronic device, which realizes one of logical functions. The series includes plenty of logical elements. On a schematic diagram a logical element is represented by a rectangle, in the middle of which the image of a parameter of function is placed. The lines from the left side of a rectangle show inputs, lines from the right side - outputs of an element. Graphics images of the most widespread values are presented in table 2.11. (Inverse inputs and circles show the outputs).

Table 2.11 - **The most used values**

Name of a valve	Graphical image	Boolean function
1	2	3
AND (conjunctor)		f=xy
OR (disjunctor)		f=x+y
OT (invertor)		f=x
AND – NOT (Sheffer stroke)		f= xy
OR – NOT (Arrow of the Peirce)		f=x+y
Exclusive OR		$f=x \oplus y$
The repeater		f=x
NOT-OR		$f=\bar{x}+\bar{y}$
AND-OR-NOT		$f=\overline{x_1y_1+x_2y_2}$

The functionality of logic elements and their physical parameters also depend on the target cascade of an element. The three types of target cascades are used more frequently. Figure 2.6, a presents the logic element with a standard output.

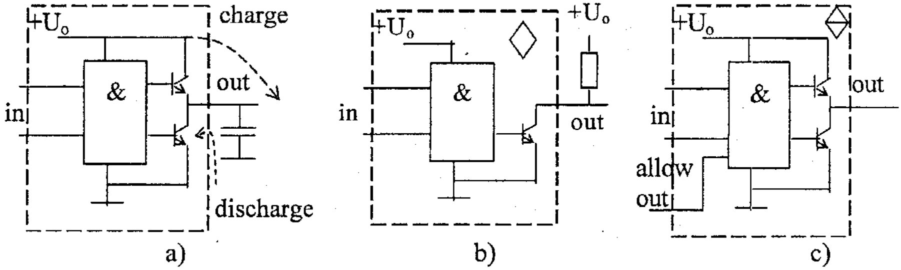


Figure 2.6 - Target cascades of logic elements

Target cascade of logic elements consists of two sequentially connected transistors, which are supervised by a logical part of an element. One of transistors is always open, and other is closed. The open transistors, having small resistance, quickly recharge the capacity of a load and parasitic capacity of hookup, therefore elements of such type have found broad application.

In a logic element with an open collector (the figure 2.6, b) the transistor is used as the target cascade, collector of which is not connected to loading. The outputs of such elements should be connected to the power supply with the help of external resistor.

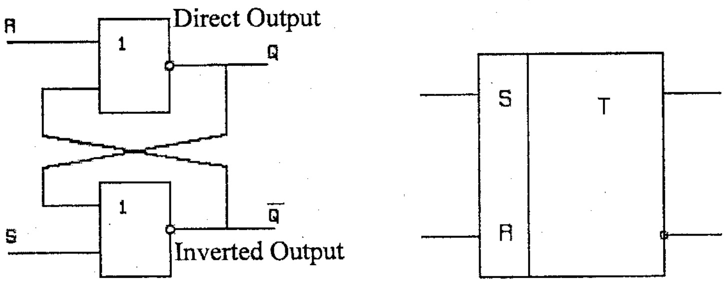
In figure 2.6, a logical element with three conditions of an output is represented: the logical element has a managing input, one from values of a signal on which translates target transistors in the closed condition, that corresponds to high-impedance state of an output (hundreds of kiloohms). The elements with three states are developed specially as the target-managing buffer for connecting digital blocks into turnpikes.

2.3.4 Triggers

As opposed to combinative logic circuits, the triggers are logic devices with memory. Their source signals generally depend not only on signals, which are applied on inputs in the given instant, but also on signals, which are applied to them earlier. Depending on properties, amount and purpose of inputs, the triggers are divided into several types [6,9]. There are clocked and unclocked triggers. The change of a state of the unclocked (asynchronous) trigger happens after an appropriate change of potentials on its controlling inputs. In the clocked (synchronous) trigger the modification of a state can be held only at the moment of presence of an appropriate signal on the clocked input. Clocking can happen by impulse (potential) or by front (overfall of a potential). In the first case the signals on controlling inputs influence a condition of the trigger only in the case of allowing potential on the clocked input. In the second case the operation of controlling signals happens only at the moment of transition one-zero or zero-one on a clocked input. There are also universal triggers, which can work both in clocked and in unclocked modes.

The general types of triggers in integrated fulfillment are named as follows: D-triggers, T-triggers, RS-triggers and JK-triggers.

The elementary unclocked **RS-triggers** (figure 2.7, a) consist of two circuits OR-NOT, closed in circle. Such trigger has two inputs: S (establishment) and R (dumping), and two outputs $\overline{Q}$ and Q. Its label on the functional schemes is shown in figure 2.7, b.



a) b)

Figure 2.7 - RS-triggers on elements OR-NOT

While on both controlling inputs R and S the levels of signals are not active, in this case equal to 0, the trigger is in one of two proof conditions. If the significance of a signal on an output Q equals 1, then, as it is shown in the scheme, this single signal, arriving on a circle of feedback on an input of the lower element, casts an emerging of a signal with zero level on an output Q. In its turn a zero level of an output Q, arriving on an input of the upper element, supports Q in condition 1. In this case it is said, that the trigger is set. By virtue of symmetry of the scheme it will be as much constant in opposite - zero state, when the level on an output Q is equal to 0 - trigger is dumped. A mode of the RS-trigger, when both controlling signals R and S are inactive, is named as a mode of preservation.

The timing diagram of transients in the circuit during the application of controlling signals on it is shown in figure of 2.8.

The output target condition of the trigger is zero. The diagram shows arrival at first of the signal S, then, after its ending - signal R. Upon termination of a source signal the trigger can keep its new condition for a long time. It is said that the trigger remembers a source signal.

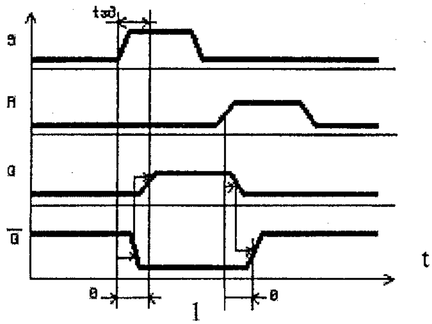


Figure 2.8 - Timing diagrams of function of the RS-trigger

If both source signals are given simultaneously new applied to the RS trigger, the zeroes will appear on both outputs Q and Q. We remove ones from inputs. R and S simultaneous both elements will begin switching to a single condition, this time each will try to keep the partner in a zero state. What element will succeed in this duel, will depend on their amplification factors, sreed of transients and other factors. The resulting condition of the trigger becomes uncertain, therefore combination R = S = 1 is considered prohibited.

RS-trigger differs from the schemes without feedback given above also by the fact, that its outputs are simultaneously its inputs. Really, if on the communication line, connected to an output Q of the trigger, which is in a zero state, the brief error will act, it simultaneously will act on an input of the lower element and can switch it, that is extremely undesirable. Therefore connection to communication lines is carried out through the buffer elements, joint by the scheme of the trigger, that increases the speed of the scheme shown in a figure 2.9. Since on inputs of the buffer trigger T2, R or S-signal is constantly present, this trigger can not remember an error any more and after its ending it will return to the correct condition immediately.

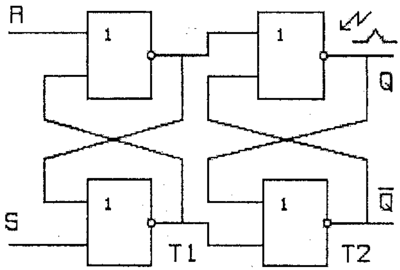
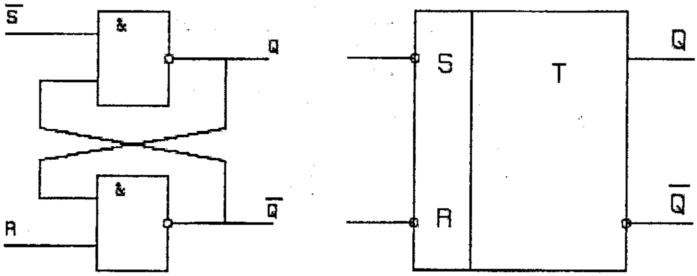


Figure 2.9 - RS-trigger on elements OR-NOT

The trigger constructed on elements AND-NOT is shown in a figure 2.10.

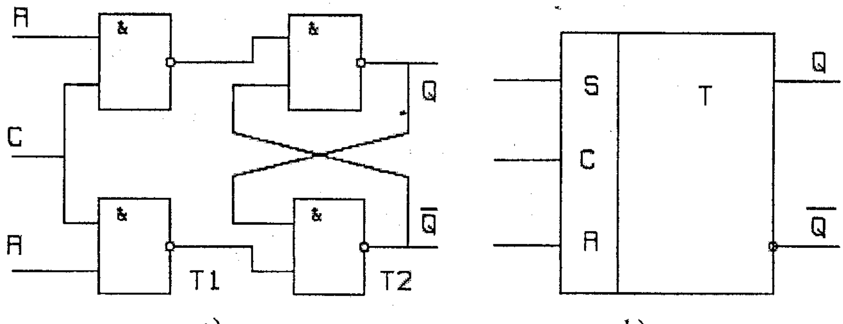
The signals of control R and S have an active low level. In a mode of preservation on both inputs there should be ones, but the simultaneous feeding of two zeroes is prohibited. In TTL-series almost all triggers are created by the scheme given in a figure 2.10, a.



a) b)

Figure 2.10 - Functional scheme (a) and graphical symbol (b) The RS-triggers on elements AND-NOT

Main purpose of triggers in the digital schemes is the preservation of the outcomes, produced by the logic schemes. For elimination of the outcomes, deformed in the transients, between an output of the logic scheme and an input of the trigger it is possible to include a conjunctor such as element C in a figure 2.11.

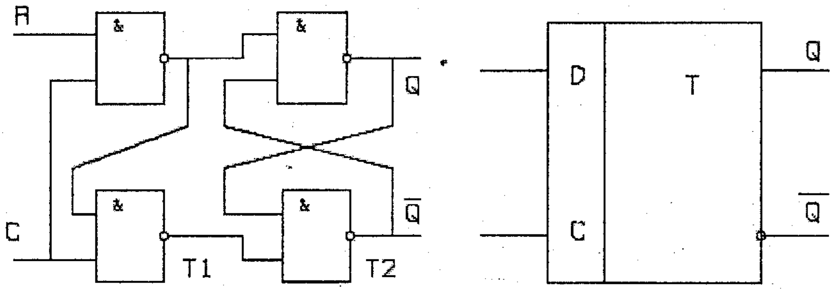


a) b)

Figure 2.11 - Synchronous RS-trigger

This solution turned to be very efficient, has become typical quickly and induced the manufacturers of triggers to include conjunctor, controlled by a synchrosignal, into the structure of the trigger. So the **synchronous triggers** appeared, which are switched to a condition, which is given by controlling inputs only upon a signal of synchronization, which arrives on synchroenter C of the trigger. In the inactive level of C-signal the synchronous trigger is in a mode of preservation and does not react on any controlling signals. The development of idea of the synchronous trigger has lead to emerging of various trigger devices.

The D-trigger (latch) is the synchronous trigger, which has two inputs: an input of data D and input of synchronization. The D-trigger is switched only by a signal on C-input and also to the state, which is specified by D-input. C-signals in this case play a role of a command to store in the trigger. One of the possible functional schemes of the single-cycle D-trigger and its graphical symbol are shown in a figure 2.12.



a) b)

Figure 2.12 - Clocked D-trigger

The diagram in a figure 2.13 illustrates the features of innovation of the D-trigger (transparent latch).

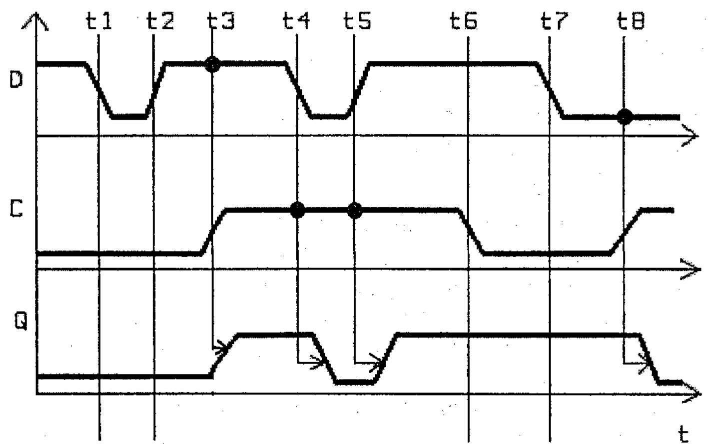


Figure 2.13 - Timing diagram of work of the D-trigger

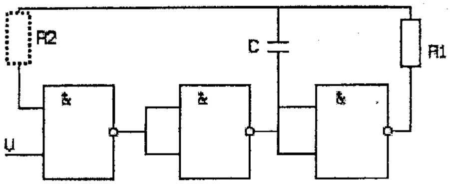
The changes of a D-input when C = 0 (moment t_1,t_2,t_7) do not influence in any way a condition of an output Q: the trigger is closed on arrival of C and is in a mode of preservation. The front of C-signal (the moment t_3) causes switching of the trigger in that condition, which was to this moment on input D. When C = 1 latch is transparent: any modification of D-input (moments t_4,t_5) causes a modification of an output Q. On a shear of synchrosignal (moment t_6) the trigger fixes on an output that condition, which was on a D-input. The following modification Q is possible only on front of the following clock pulse (moment t_8). If on C - input is given a constant single impulse, a property of memory of latch will not be exhibited in any way, and it will also execute functions of the usual buffer power amplifier in a tract of data transfer. If an input D of the trigger (figure 2.12) is connected with its inverse output ($D = \overline{Q}$), each overfall on its clock input will result in transition of the trigger in an opposite state, the frequency of a signal on an output of the t-trigger is twice lower than frequency of a signal on an input therefore such trigger can be used as a divider of frequency and binary counter.

In a series of chips, which are issued there are also universal **JK-triggers**, which, with an appropriately connected source logic, can execute functions of triggers of any other types. The JK-triggers represent sequential regenerative bistable devices with two information inputs J and K, which in the case of a source combination J=K=1 switch the trigger in an opposite condition similarly to the t-trigger, and upon any other combinations they work as the RS-trigger, in which the role of inputs S and R is executed by appropriate inputs J and K: $J \equiv S, K \equiv R$

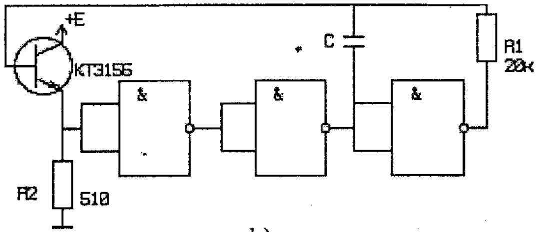
2.3.5 Use of digital elements in impulse circuits

Direct purpose of digital IC is to execute different logical functions. However in reality digital and analog-digital electronic devices contain, as a rule, auxiliary impulse junctions - generators and shapers of impulses. These impulse junctions can be made under the traditional schemes on the basis of discrete electronic elements (transistors, diodes etc.). The special integrated schemes can also be used.

Generators of impulses, during the construction of which on the basis of digital IC the intensifying properties of inverters are used. To ensure the generation and support of the steady auto-oscillations, it is necessary at first to introduce inverters on direct current to a linear plot of transfer performance - plot between levels «zero» and «one», where the inverters work as inverting amplifiers of a source signal. After that it is necessary to add into the system a positive feedback with the help of one or two condensers. Figure 2 presents 14 the schemes of thus constructed multivibrators. The stabilization of modes of inverters on direct current is ensured in this case at the expense of general feedback through the resistor R_1, which envelops three sequentially connected inverters. The positive feedback will be realized at the expense of the condenser C. Feeding V in the multivibrator figure 2.14, a is used to stop the generation of impulses.



a)



b)

Figure 2.14 - Schemes of multivibrators on the basis of logical inverters

For this purpose it is necessary to give on input V a signal «zero» in the device. The period T of impulses, which are generated by the multivibrator, is determined by a constant of time $\boldsymbol{\tau=R_1C}$. With the use of TTL-inverters the resistance R_1 can be within the limits from 0 up to 2 kOhm, KMOH - from 10kOhm to 10MOhm with installation of the bounding resistor $R_2=R_1$.

Rather large source currents of TTL-inverters do not allow increasing resistance of the resistor of feedback R_1. Therefore for receiving of low-frequency impulses it is necessary to use the great capacity C. For reduction of the capacity it is possible to supplement the inverter of the multivibrator by the emitter repeater, as it is shown in figure 2.14. The resistance of the resistor R_1 can be enlarged in this case up to 10. .20 kOhms.

The **generators of impulses** can be constructed on two or even on one inverter (figure 2.15).

In the generator on scheme 2.15, the resistor R1 brings in an intensifying mode to the first inverter, and its voltage output is supported in a mode of amplification by the second inverter. In this case positive feedback through the condenser C causes soft (does not require an initial push) self-excitation of self-oscillating relaxational process. As the second inverter is not enveloped by feedback on a direct current, the device appears more critical in relation to resistance R_1, than multivibrators on three inverters. Upon the use of TTL-inverters usually R_1=0,2...2 KOhms. Upon use of KMOH-inverters, this resistance can be changed from several tens of KOhms up to several MOhms. To increase the stability of the mode of the second inverter on direct current, it can be supplemented with resistor feedback (figure 2.15, b).

The generators on KMOH-inverters can be constructed with quartz stabilization (figure 2.15, c). In low-frequency quartz generators (10...100kHz) it is recommended to connect the inputs of inverters with the ground with the help of small capacities to destroy parasitic high-frequency generation.

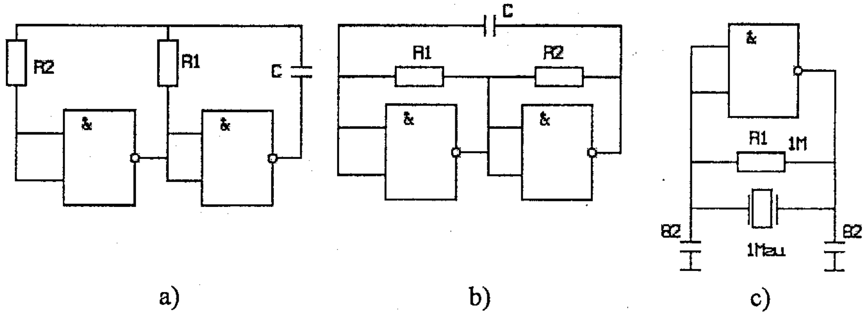


Figure 2.15 - Schemes of generators of impulses on the basis of inverters

The formers of voltage of the rectangular form are used for receiving the target signal, which accepts only two standard levels -1 and 0, from any source signal. In the shaper (figure 2.16) positive feedback is executed through the resistor between an output of the second inverter and input of the first.

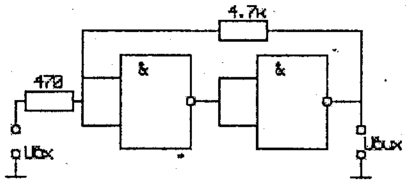


Figure 2.16 - Former of voltage of the rectangular form

The source voltage moves through the additional resistor (470 Ohm), which resistance also influences the depth of positive feedback. The increase of resistance of the resistor increases factor of positive feedback and reduces sensitivity of the shaper to source voltage.

As the formers of signals with standard levels the triggers of Smitt, D-triggers and special integrated circuits of formers (TL) can be used.

Formers of impulses of specific duration (single-vibrators) ensure receiving of target impulses upon appropriate overfall of a source signal. Some variants of the schemes of one-vibrators constructed on digital ICs, are shown in a figure 2.17.

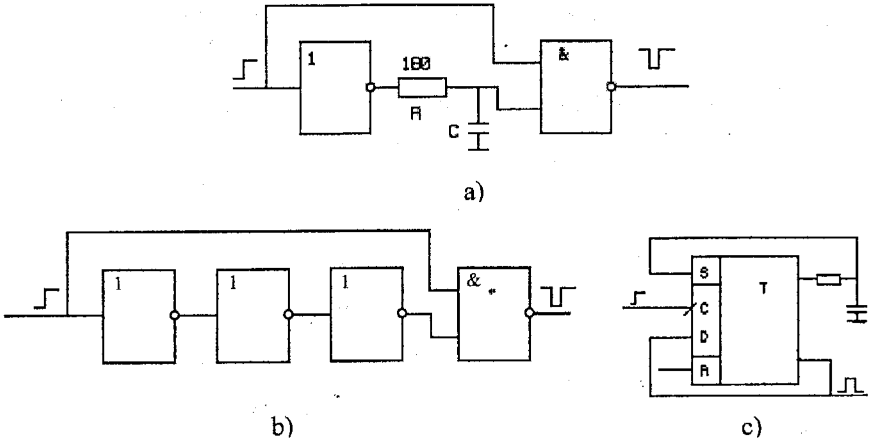


Figure 2.17 - Schemes of one-vibrators on ICs

In the one-vibrator figure 2.17, on inputs of the second inverter the mutually inverse signals from an input and output of the first inverter are fed, therefore in the static mode signal on an output of the device is always equal to one. The signal «zero» on an output of the second inverter occurs only in the case, when the signal on an input of the first inverter passes from a zero to one. The switching of the first inverter take place on both inputs of the second the signals «one» will be sent. The duration of target impulse of shaper can be increased, increasing time of switching of the first inverter, by connecting to its output of a RC-circuit.

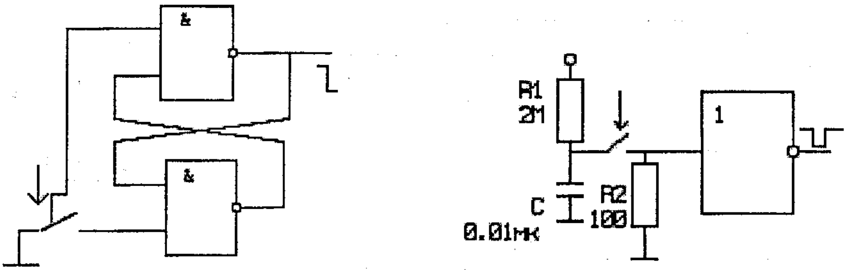
The duration of target impulse of one-vibrator can also be increased, including some inverters between an input of the device and target inverter (figure 2.17, b). It is necessary only to remember, that an amount of inverters should be unpaired.

The more steep fronts of target impulse are ensured with one-vibrator on the basis of trigger, timed by front (figure 2.17, c). The overfall 0/1 on a clock input of the trigger installs it in the state 0. After some time necessary for the discharge of the condenser, on an output of a RC-circuit, connected to the trigger, also appears a signal «0». This signal, acting on an input of the trigger S, returns it in the condition «1».

The one-vibrators are produced also as the ready integrated circuits.

The formers of impulses from mechanical contacts solve the problem of shaping of precise transition (0/1 or 1/0) or short impulses upon operation of the relay or other mechanical switch. The specificity of such switch is that its operation is accompanied by the chatter of contacts (repeated transition during a short time from the closed condition to breaked and back). It can lead to forming of a pack of impulses instead of desirable single impulse or overfall of a potential. Figure 2.18 gives the examples of the schemes of shapers, which eliminate this undesirable effect.

The shaper (figure 2.18, a) represents the elementary trigger on elements AND-NOT. The signal «zero», which is applied with the help of switches to one of inputs of this trigger, overturns it. Upon each operation of the switch



a) b)

Figure 2.18 - Schemes of formers with start from mechanical contacts

the trigger reacts to the first closure of an appropriate contact pair and the following vibration does not change any more its condition.

Upon the closure of the switch (figure 2.18, b) the condenser is quickly discharged through the resistor R2. Not overfall, but impulse is produced on an output of the shaper. One more method of forming of single impulse upon operation of mechanical contacts is the use of one-vibrator, length of impulse of which is installed greater, than probable time of chatter of contacts.

2.3.6 Rule of circuit inclusion of elements

During the development of the schemes, a maximum allowable target current and the capacity of a load are stipulated frequently besides an output capability and that is necessary to know during the docking of various elements.

The unused inputs I in majority of a series should remain not connected. In TTL and TTLS-series the signal from free inputs is treated as logic one, and in elements AND-NOT it would be possible to keep it free, however additional charges in basis, originating in them, decelerate switching an element on other working inputs. Therefore unused inputs are integrated with others, if upon this the safe load of a source of signal is not exceeded, or they are connected to a source of logic one. As the second one the element AND-NOT is used, which input is grounded, or resistor with resistance 1 COMAS, connected to the power supply + 5B. It is possible to connect to one such a resistor up to 20 unused inputs I.

In CMDS-elements there should not be unconnected inputs at all, as any potential can appear on them, accordingly this signal will appear on the output. The unused inputs can be connected to the power supply directly, without the resistor or they can be integrated with the working inputs.

The unused inputs OR in any series should be connected to a logic zero, namely with a general wire. In the unused section OR of element AND-OR-NOT, all, or at least one input AND should be connected to a general wire.

If some elements, which are included into structure of the case, are not used, then on inputs of the unused elements of a TTL-series it is necessary to feed such signals. Which have "one" on their output on such condition the element consumes less power and it can be used as a source of logic one. The unused elements of a CMDS-series can be fixed in any state, only not to keep them in an undefined state.

The outputs of elements with usual target cascades are forbidden for integration, that the initial developers sometimes tried to make for getting an "collection" (logic OR) of two signals. It will lead to damage of target transistors. Especially it is impossible to connect outputs of elements to a general wire or bus of a feed.

The elements with an open collector in difference from usual logic elements are adapted to connection on an output (scheme of assembly OR). The principle of assembly OR is widely used in memory LIS and PLA, and also for construction of bi-directional numerical buses (turnpikes).

2.4 Junctions of digital equipment

2.4.1 Registers

The registers are devices intended for reception, preservation, simple transformations and transfer of binary numbers. Simple transformations imply a displacement of numbers on specific amount of the positions, and also transformation of a sequential binary code in parallel and back. Base elements of the registers are the triggers, which are supplemented by combinative logic elements for realization of various connections between the positions of the register and for management of a reception and transfer of operands. A main functionality of the registers is random access memory for multidigit binary numbers.

Depending on the method of reception and transfer of binary information, there are sequential, parallel, sequentially parallel, parallel-sequential and universal registers.

In the parallel registers or registers of memory the input/output of all positions of number is carried out simultaneously during one step. For construction of the n-digit register of memory it is necessary n of triggers. The parallel registers are the main functional elements for construction of operating storage devices.

In the sequential registers the input/output of information happens through one information input and one output with a displacement of number. Therefore sequential registers are named as the registers of displacement. For one step information, which is entered and taken out, is shifted on one category to the right or to the left. The registers of displacement, which will realize on command the displacement management of information to the right or to the left, are named reversible.

Sequentially parallel registers have one information input for sequential input of number in the mode of displacement and target valves for issue of n-digit number by parallel code. Such registers execute transformations of a sequential code in parallel.

In the parallel-sequential registers the information is entered by a parallel code for one step through clock ingates, and is removed from them sequentially under one position in each clock interval. In an outcome the operation of transformation of a parallel code to sequential is realized.

The universal registers have possibilities of all types of the registers and, besides, ensure a mode of a cut-off of inputs and outputs (third logical condition) of a register from a general information bus, recommutation with places of inputs and outputs of the register and by that switching of functions of a reception/transfer of information in a general information bus.

The technical parameters of the registers are determined by parameters of their main functional junction — trigger and by digit capacity of an operand. As an example we shall consider the parallel register (figure 2.19, a) and moving register (figure 2.19, b) on the basis of D-triggers.

In the parallel register the input of information takes place on an interval of synchronization C=0. The target logic elements form target signals according to expression

$$Y_i = P\bar{Q}_i + P\bar{q}_i,$$

that is when P=1, Y_i=Q_i the information from the register is issued in a true form, and when P=1, Y_i=Q_i - in the inverted code.

The input of information in the sequential register can happen sequentially from an input X with a consequent displacement of information to the right on one position on each clock pulse C or in parallel from inputs A on a signal I=1 of asynchronous notation of number to the previously cleared register (R=0). Upon closure of outputs of the sequential position with a sequential input (the dashed line) the ring moving register is realized, which is convenient for using for construction of, for example, clock generators of digital systems.

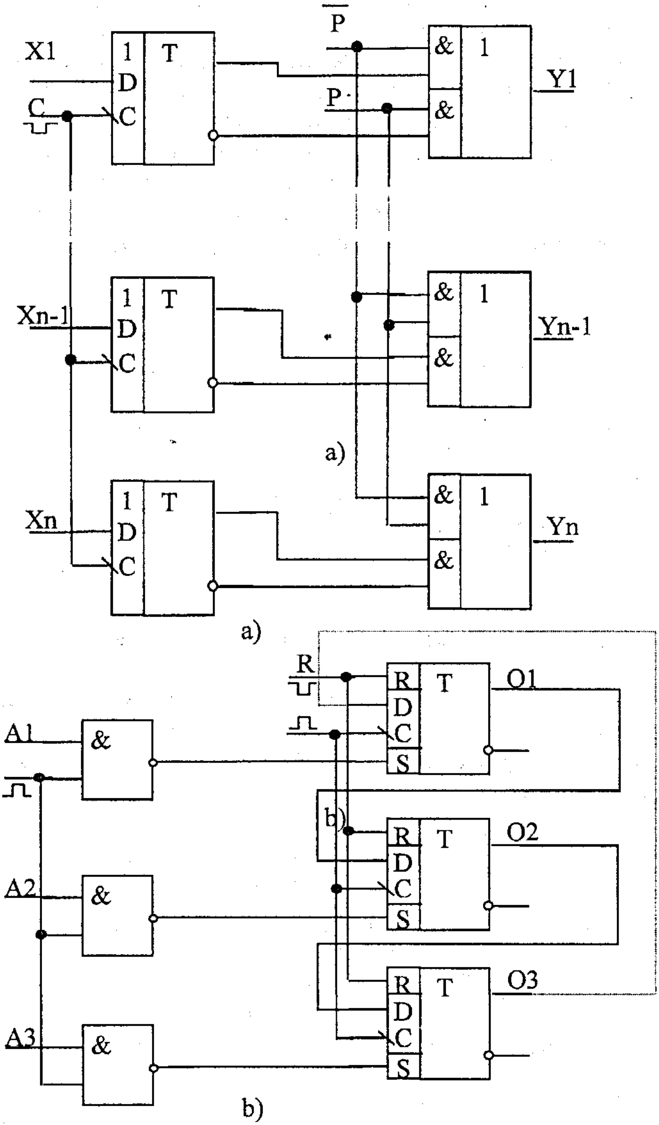


Figure 2.19 - Parallel (a) and sequential (b) registers on the basis of D-triggers

2.4.2 Counters

The counter is the digital system intended to count and store an amount of impulses, fed in the certain time frame on its accounting input. By a type of the counter condition modification by accounting impulses there are distinguished summing, subtracting and reversible counters. The amount of various conditions of the positions of the counter is an indication for a classification, according to which counters are named binary, binary-decimal etc. Except for accounting input counters can still have inputs of asynchronous or synchronous installation of an initial condition. In asynchronous counters the synchronization and the transition of the positions in a new condition, common for all positions, is absent and happens sequentially, category by category (figure 2.20).

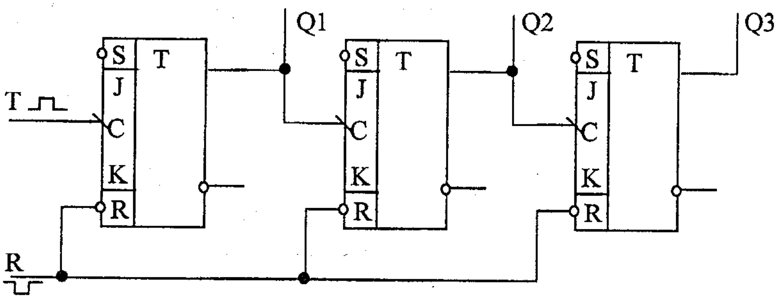


Figure 2.20 - Asynchronous counter

The main drawback is low speed, which is lower when there are more factors of the account. One of methods of improving speed of asynchronous counters is the organization of transitions between the position through additional logic elements (figure 2.21).

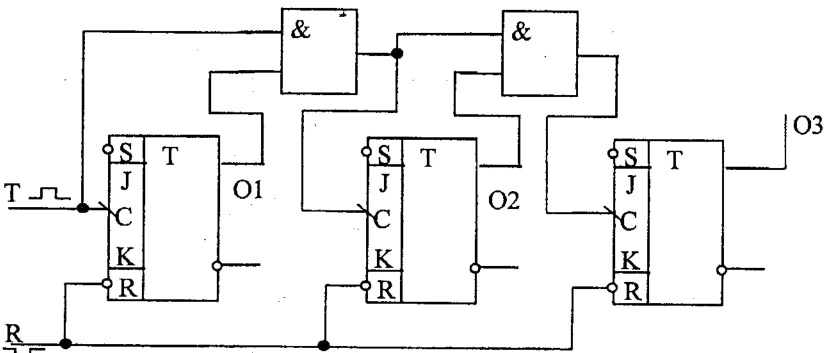


Figure 2.21 - Asynchronous counter

These counters concern to asynchronous counters, at which the switching of the positions happens simultaneously, irrespective of remoteness of the position from an accounting input. The scheme of the elementary summing asynchronous counter is given in a figure 2.22.

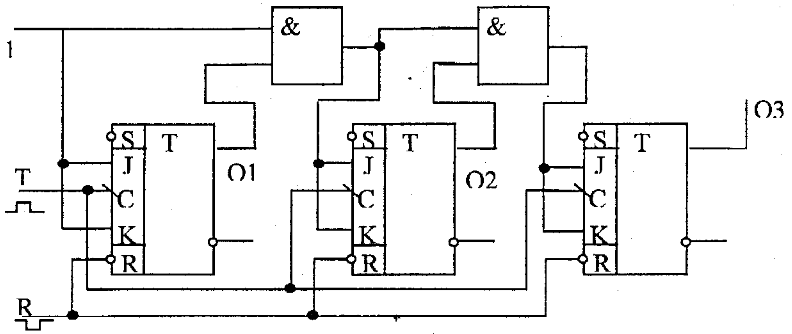


Figure 2.22 - Synchronous counter

The principles of construction of synchronous and asynchronous reversible counters are similar: the direct count will be realized by turning on carry circuits from single outputs of triggers of rightmost on inputs of top digits, and feedback (subtraction) - by turning on circuits of borrow between inverse outputs of triggers of rightmost and inputs of top positions.

2.4.3 Converters of codes

The converters of codes are intended for transformation of numbers from one form to the other. For example, to enter information in the ECM it is necessary to convert decimal numbers in binary, and during an output of information to the indicator or printing station binary or bcds are converted into codes of management of the character generator, light-emitting diodes or liquid-crystal display panels, mechanism of printing.

As an example we shall construct a converter of code 8421 in the code of the seven-segment indicator. If the segments are designated by the letters, as shown in a figure 2.23, table 2.12 shows the correspondence between binary-decimal number and a group of segments, necessary for display of decimal digit.

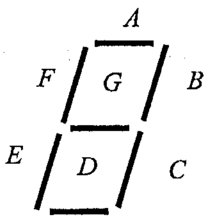


Figure 2.23 - Seven-segment indicator

Table 2.12 - **The table of the correspondence**

Decimal number	**Code 8421**				**Seven-segment code**						
	d	**c**	**b**	**a**	**A**	**B**	**C**	**D**	**E**	**F**	**G**
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

The segment A is determined by a set of code 8421 as follows:

A =

dc \ ba	**00**	**01**	**11**	**10**
00	1	0	1	1
01	0	1	1	1
11	*	*	*	*
10	1	1	*	*

$d + b + ac + \bar{a}\bar{c} = \overline{ac} * \overline{\bar{a}\bar{c}} * \bar{b} * \bar{d}$

Similarly we shall receive the Boolean expressions for other segments:

$\mathbf{B} = ab + \bar{a}\bar{b} + \bar{c} + \bar{d} = \overline{\overline{ab} * \overline{\bar{a}\bar{b}} * c * \bar{d}}$;
$\mathbf{C} = a + \bar{b} + c + d = \overline{\bar{a} * b * \bar{c} * \bar{d}}$;
$\mathbf{D} = \bar{a}b + b\bar{c} + \bar{a}\bar{c} + a\bar{b}c + \bar{d} = \overline{\overline{\bar{a}b} * \overline{b\bar{c}} * \overline{\bar{a}\bar{c}} * \overline{a\bar{b}c} * d}$;
$\mathbf{E} = \bar{a}b + \bar{a}\bar{c} + \bar{a}d = \overline{\overline{\bar{a}b} * \overline{\bar{a}\bar{c}} * \overline{\bar{a}d}}$;
$\mathbf{F} = \bar{a}\bar{b} + \bar{a}c + \bar{b}c + d = \overline{\overline{\bar{a}\bar{b}} * \overline{\bar{a}c} * \overline{\bar{b}c} * \bar{d}}$;
$\mathbf{G} = \bar{a}b + b\bar{c} + \bar{b}c + d = \overline{\overline{\bar{a}b} * \overline{b\bar{c}} * \overline{\bar{b}c} * \bar{d}}$.

Accordingly, by identical expression it is possible to receive various variants of a converter. In a figure 2.24 one of possible variants of a converter on elements AND-NOT is represented.

One of the cases of a code converter is the **encipherer** – a device, which ensures issue of the certain code in reply to excitation of one of inputs. The encipherers are widely used for transformation of decimal digits and alphabetic symbols in binary code during an input of information in the ECM and other digital devices.

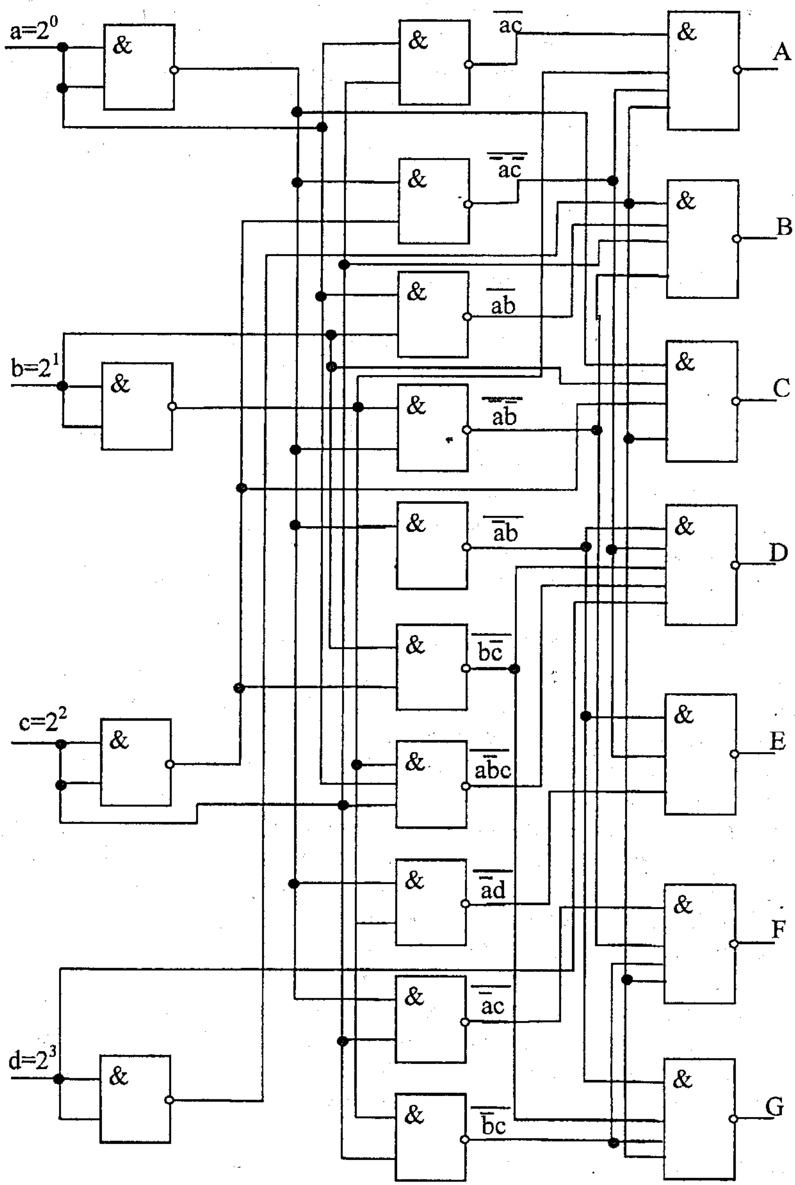


Figure 2.24 - Converters of a code 8421 in a code of the seven-segment indicator

The reconversion of a binary code into the code "1 of n " is executed by converters of the code, which are named as decoders. Decoders are widely used in devices of output of information from the ECM and other digital devices on peripheral equipment of visualization and documentation of alphanumeric information. For this purpose it is necessary to give a signal on one of n, for example of cathodes of the gas-discharge indicator or elements of selection of symbols of a printing station.

2.4.4 Semiconducting storage devices

Storage devices (SD) are used for preservation of information and exchange with other parts of the ECM or microsystems. By functionality SD are subdivided into external, buffer and internal.

The external SD are used for preservation of large quantities of information and software of a system. They use the SD on magnetic disks.

The buffer SD are intended for intermediate data preservation during an exchange between external and internal memory.

The external SD are divided by functions on operating and constants.

The operating SD (RAM) execute an entry, preservation and reading of any information.

The constant SD (ROM) execute preservation and issue of a constantly noted information, the structure of which does not change in operating time of a system. By method of information filing, ROMs are subdivided on ROMs, which are programmed at factory-manufacturer; programmable ROM (PROM); programmable single-validly by user; reprogrammable ROM (RPROM); programmable multiply by user.

By method of preservation of information RAM is divided into static and dynamic. The storage elements of static SD are bistable elements, which ensure reading information without its destruction. In dynamic SD for preservation of information the inertial properties of reactive elements (condensers) are used which require periodical regeneration of information.

The classification of the SD is shown in figure 2.25.

Main parameters of the SD are: an information capacity (M) and speed.

The information capacity characterizes an amount of information, which can be stored in a storage element, and is determined by bits or amount of words N with the indication of their digit capacity n. For example, 1x256, 4x1024, 8x1024.

The speed is characterized by the time of access and write cycle. Time of access $t_{в}$ - a slice of time between a moment of feed of a selection signal and emerging of an information on an output of a chip of the SD. A write cycle $t_{ц.з.}$- minimum allowable time between a moment of feed of a signal of selection upon writing and moment of a beginning of the following operation of reading (writing).

By the structure the semiconducting RAMs, PROM, RPROM (figure 2.26) and ROM (excepting writers) consist of the following typical junctions: an accumulator HK; a decoder of lines and columns DCX, DCY; writer ROM DW; device of reading of the ROM DR; control unit CU [3].

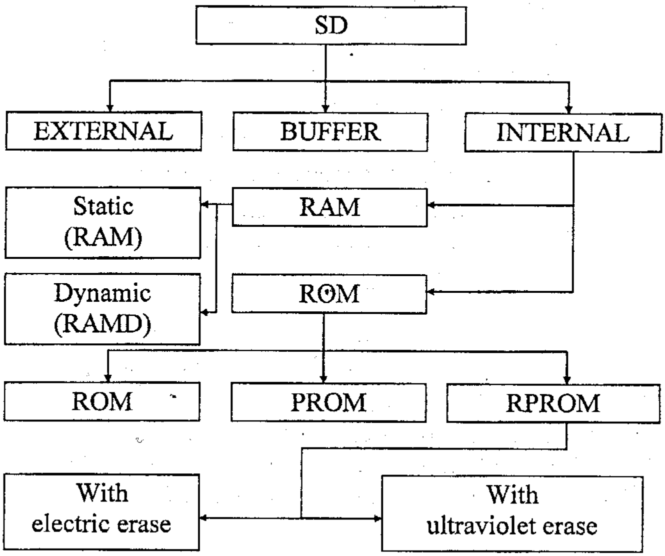


Figure 2.25 - Classification of the SD

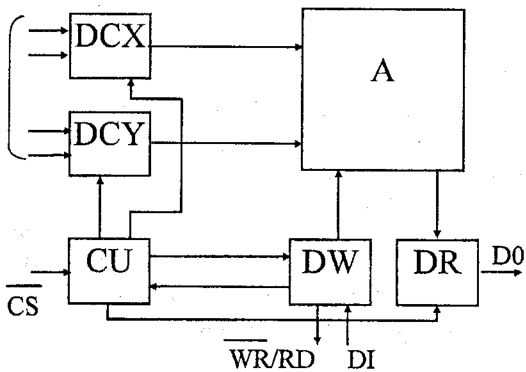


Figure 2.26 - Structure of the SD

The timing diagrams of work of the SD are represented in a figure 2.27.

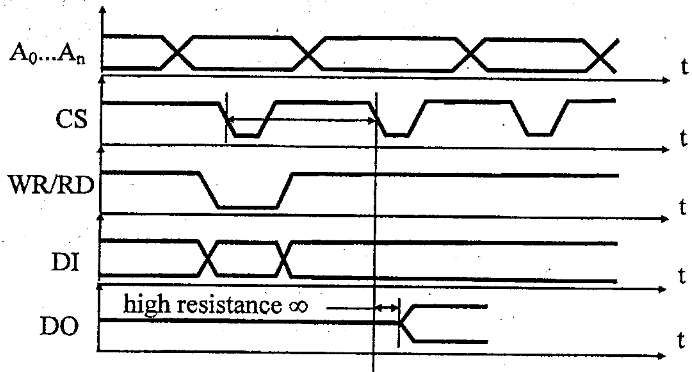


Figure 2.27 - Timing diagrams of work of the SD

The accumulator is a matrix of storage elements, integrated to lines and columns through untying key elements connected by decoders.

Diodes, bipolar transistors and МДН-structures, amorphous semiconductors and others are used as state elements

The schemes of main storage elements (SE), on the basis of which ROM and PROM are developed, are displayed in a figure 2.28.

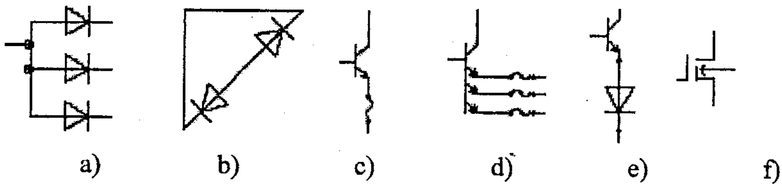


Figure 2.28 - Schemes of main SE

For ROM with accumulation on SE (figure 2.28, a, e) the entry of information is expected by two methods: by modification of a configuration of metal wiring layout (photo mask) or selective cover of contact windows under bonding (by laser ray). For PROM SE (figure 2.28, c, d) are programmed by smelting of fusible cross connections, and SE (figure 2.28, d) are programmed by method of vibrating destruction of diodes.

2.4.5 Programmable logic arrays

Programmable logic arrays (PLA) as well as PROM concern to programmable IC of a two-stage structure, which consists of two sequential matrixes "Matrix AND - matrix OR" [3]. PLA differ from PROM by the fact that in PROM a matrix AND is rigid, and matrix OR is programmed, and in PLA both matrixes are programmed. The block diagram of PLA (figure 2.29) consists of source and target buffer cascades $Б_{вх}$, $Б_{вых}$ and matrix of elements AND and OR (M_i-M_1, M_{or}-M_2). The source buffers unload source circuits and convert single-phase source signals in paraphase.

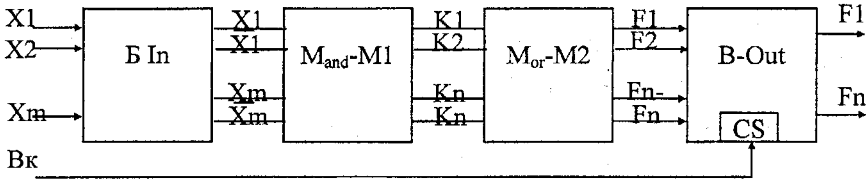


Figure 2.29 - Block Diagram of PLA

The target buffers ensure a necessary output capability of PLA and gate it with the help of input of selection of crystal SC, the signal on which either allows the work of PLA, or transfers outputs in a condition "switched off". Main parameters are the amount of inputs m, amount of transitional circuits (terms) L and amount of outputs N. The structure of a matrix AND and OR consists of horizontal and vertical buses, in junctions of intersection of which there are elements of communication, which are entered or destroyed during programming (figure 2.30, a). SE, for example, the diodes in a matrix AND (figure 2.30, b), and transistors in a matrix OR (figure 2.30, c) can be considered as elements of communication.

PLA as well as PROM are widely used for realization of switching functions Fn, for the transformation of codes, and as the control storage of the ECM with microprocessor management.

2.4.6 Display units

The display of a source and target information of digital systems largely determines their ergonometrical parameters and influences productivity of an operator. All display units are in general used for indication, visualization and documenting. The alphanumeric printing systems and other concern to the latter. The devices of indication ensure operating display of an information. It is created on the basis of various optical devices, electron-beam tubes, incandescent lamps, luminodiodes, gas-discharge, electroluminescent, mesomorphic indicators. The elementary display units in digital systems are luminodiodes and digital indicators.
Luminodiodes can be used for indication of levels on an output of chips of TTL and transistor cascades. Luminodiode can shine upon low (figure 2.31, a), as well as upon high (figure 2.31, b) levels of a signal on an output of a chip.

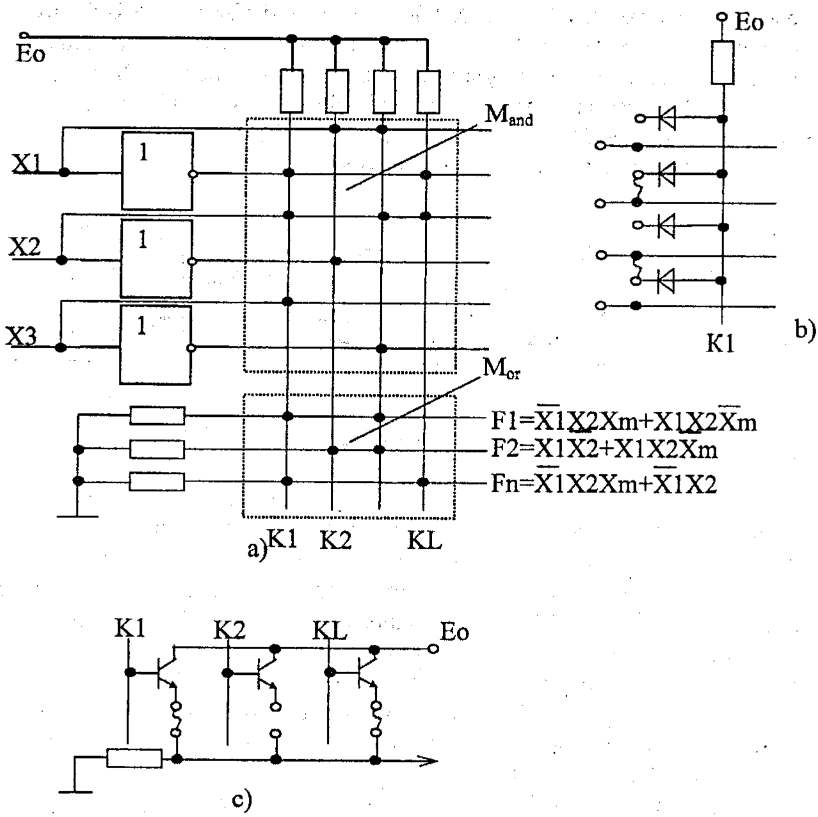


Figure 2.30 – Structures of a matrix AND and OR

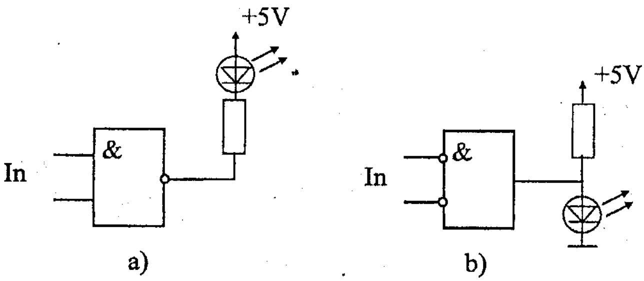


Figure 2.31 - Schemes of activation of luminodiodes

The greatest use among digital display units have received seven-segment and matrix luminodiode indicators.

Methods of forming of luminodiode signs with the help of seven-segment indicator are shown on a figure 2.32-2.33.

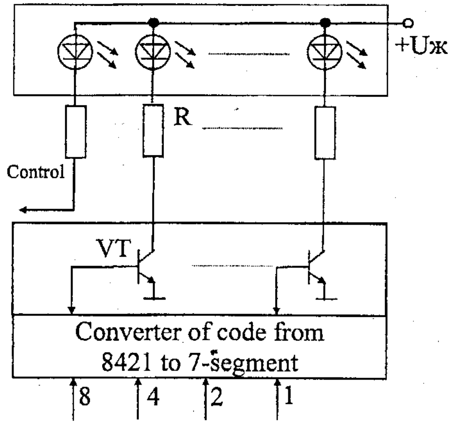


Figure 2.32 - Methods of forming of luminodiode signs

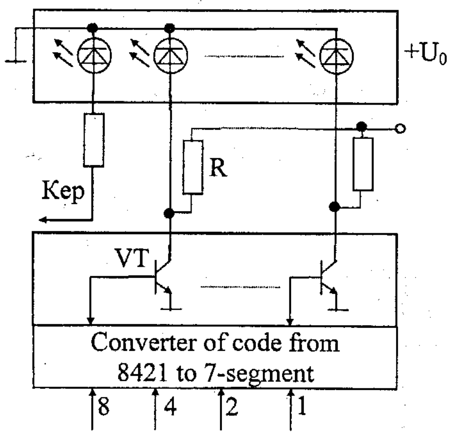


Figure 2.33 - Methods of forming of luminodiode signs

Multibit indicators constructed by the scheme in a figure 2.31, have the increased costs of equipment, which will increase in proportion of digit capacity N of number on the indicator. The costs of equipment can be reduced, if instead of simultaneous (parallel) indication of all N categories to proceed to separate (sequential) indication (figure 2.34).

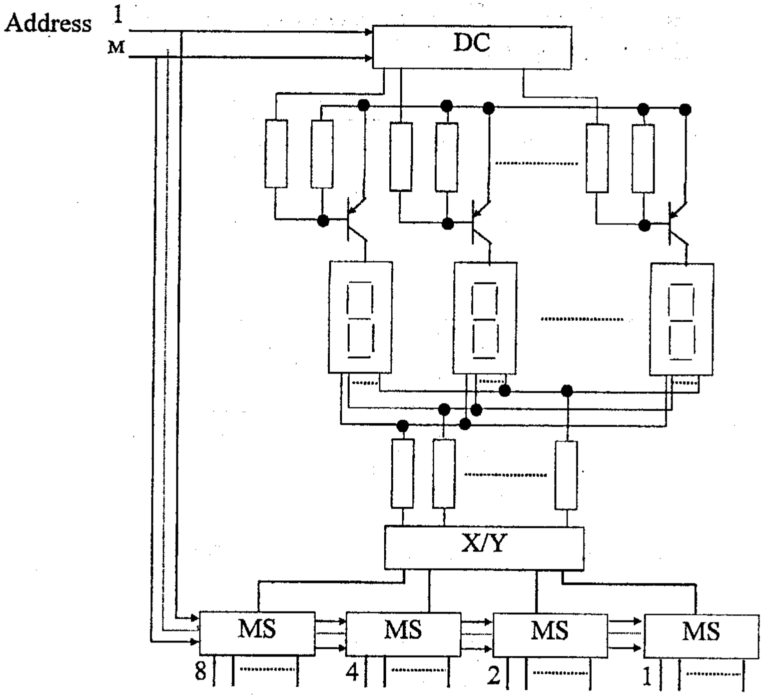


Figure 2.34 - Sequential indication of digits

The scheme of matrix luminodiode indicator is shown on figure 2.35.

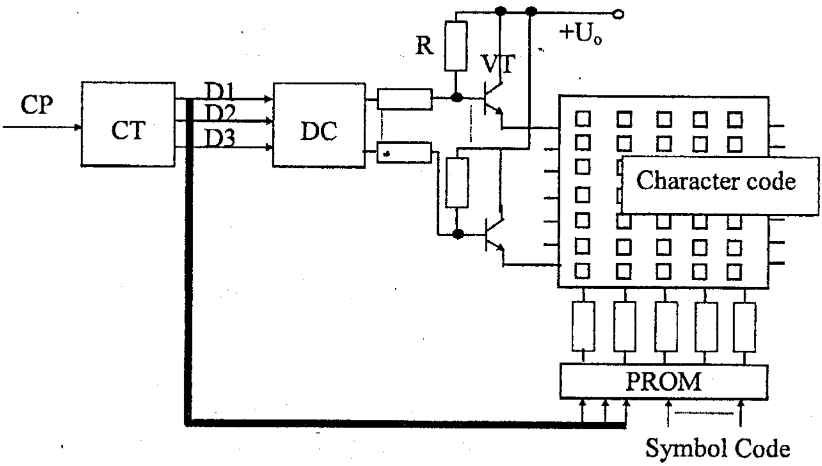


Figure 2.35 - Scheme of matrix luminodiode indicator

The clock pulses (CP) arrive on the three-digit counter, its target signals determine a code of a line and arrive on a decoder, and as a part of a code - on ROM. One of transistors VT, the base of which through the resistor R from a decoder the level of logic "1" arrives, is opened and connects emiters of luminodiodes (line) to a power supply unit $+U_0$. Upon it diodes of columns, on which from ROM the zero levels are presented, radiate light.

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Навчальне видання

Роман Наумович Квєтний, Сергій Григорович Кривогубченко,
Денис Сергійович Кривогубченко, Ілона Віталіївна Богач,
Микола Григорович Прадівлянний

ІНТЕГРАЛЬНА СХЕМОТЕХНІКА

Навчальний посібник

Оригінал-макет підготовлено І.В.Богач
Редактор В.О.Дружиніна

Навчально-методичний відділ ВНТУ
Свідоцтво Держкомінформу України
серія ДК №746 від 25.12.2001
21021, м.Вінниця, Хмельницьке шосе, 95, ВНТУ

Підписано до друку 7.11.2005 р.
Формат 29,7 ×42 ¼
Друк різографічний
Тираж 85 прим.

Гарнітура Times New Roman
Папір офсетний
Ум. друк. арк. 3.06

Зам. № 2005-180

Віддруковано в комп'ютерному інформаційно-видавничому центрі
Вінницького національного технічного університету
Свідоцтво Держкомінформу України
серія ДК №746 від 25.12.2001
21021, м.Вінниця, Хмельницьке шосе, 95