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Capacitively-Coupled Chopper Amplifiers

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Chapter 1
Introduction

1.1 Problem

In many measurement situations, the signal of interest is small, possibly in the range of tens of microvolts, and is superimposed on a much larger DC common-mode (CM) signal, possibly in the range of several volts. Coping with such a large CM signal and at the same time accurately measuring such small signals is a big challenge for interface circuits. A good example of such a measurement is in high-side current sensing [1], as shown in Fig. 1.1, where the load current of a battery is monitored by inserting a small sensing resistor R_{sense} in series with the battery. Thus, the current can be determined from the DC voltage drop V_{sense} across the resistor. To minimize its power consumption, R_{sense} is usually very small (hundreds of milliohm) and thus, V_{sense} is also small, typically ranging from tens of microvolts to hundreds of millivolts. This requires a readout amplifier with low offset and low $1/f$ noise. Moreover, V_{sense} is accompanied by a large CM voltage, which can be as large as 30 V in the case of a laptop battery. This is far beyond the supply voltages of normal CMOS circuitry. Thus, novel circuit techniques to reject this large CM voltage and accurately measure V_{sense} must be found. This problem becomes more challenging as CMOS technology advances, since this has historically been accompanied by a steady decrease in supply voltages.

1.2 Traditional Solutions

When a large input CM voltage must be rejected, the best solution is to block it. A first approach involves the use of a magnetic coupling [2–5]. The basic block diagram [2] of a readout system employing magnetic coupling is shown in Fig. 1.2. It consists of an input and output modulator, a transformer, and a readout amplifier. In this case, the modulators are implemented as choppers, i.e., polarity-reversing

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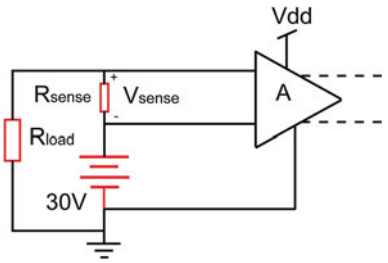

Fig. 1.1 A simplified schematic of a high-side current-sensing readout circuit

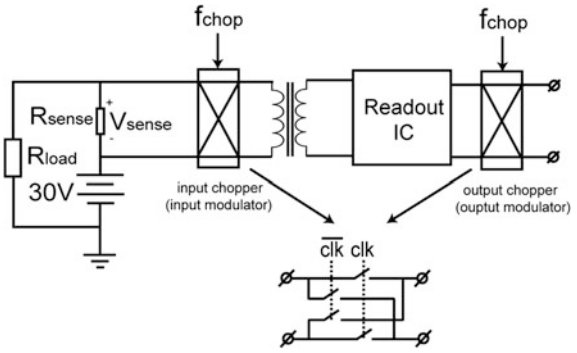

Fig. 1.2 A schematic of magnetic isolation readout circuit for current-sensing application

switches driven by a digital clock signal with a fixed frequency (f_{chop}) [6–9]. In [2], the choppers are also driven via an isolating transformer. The input chopper converts the DC differential voltage V_{sense} into a square wave, and the output chopper converts the amplified square wave back to DC. In this way, the differential signal is first modulated to high frequency by the input chopper and so can be coupled to the input of the readout amplifier via a transformer. The DC CM voltage, however, will not be modulated and thus will not be coupled to the readout amplifier. Furthermore, the offset and 1/*f* noise of the readout amplifier will be up-modulated by the output chopper and so can be filtered out. A big disadvantage of this approach, however, is that transformers are difficult to integrate on chip. Although integrated microtransformers [2] can be realized in some processes, they tend to occupy a lot of chip area.

A second approach involves isolating the DC CM voltage optically, e.g., with an opto-isolator [10–13]. Although there are many types of opto-isolator, the most common type simply consists of an LED and a photodiode as shown in Fig. 1.3. The LED is connected to the input signal and converts it into an optical signal, which is then picked up and converted back to an electrical signal by the photodiode and a readout amplifier. In this way, the input CM voltage is completely isolated from the readout amplifier. The main disadvantage of this approach, however, is its lack of accuracy. The signal transfer function between the LED and the photodiode depends on several parameters such as the voltage-to-light transfer

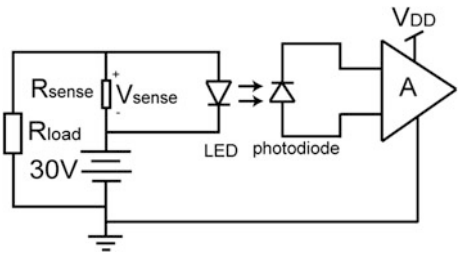

Fig. 1.3 Schematic of CM isolation with opto-isolator

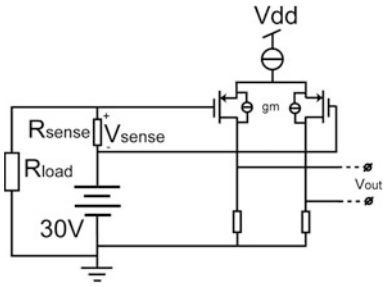

Fig. 1.4 CM isolation with basic differential pair

function of the LED, the intensity of the light picked up by the photodiode, and the light-to-voltage transfer function of the photodiode. These parameters can be difficult to control and reproduce accurately in large-scale production. Thus, the accuracy of the measurement, especially the system's overall gain, is not well defined. Moreover, the linearity of the signal is often low, which requires an extra feedback circuit [4].

A third approach, which is the most commonly used, is to isolate the CM voltage electrically. A simple way to do this is to use the basic differential pair shown in Fig. 1.4. Neglecting circuit non-idealities, the input differential pair acts as an ideal voltage to current converter, which floats between the tail current source and a potential close to ground. Since it is only sensitive to the input differential signal, the CM signal is completely isolated from the rest of the circuit. In reality, however, circuit non-idealities such as mismatch will significantly decrease the measurement accuracy. To improve this, the chopping technique can again be applied as shown in Fig. 1.5. Since the input chopper only modulates the differential input signal, its contribution to the output voltage is separated from that of the CM signal in the frequency domain. The offset and $1/f$ noise are also up-modulated and so are removed from the base band. However, the maximum CM voltage that can be handled is determined by the differential pair's supply. So handling a large CM voltage requires a large supply voltage and, consequently, high-voltage input transistors in the input stage. This increases the power consumption considerably [14, 15]. Moreover, the limited output impedance of the input transistors will reduce the circuit's CM immunity, while their offset and $1/f$ noise will reduce its DC

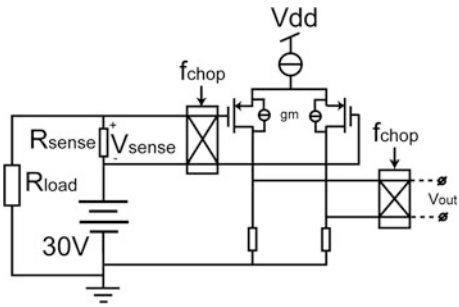

Fig. 1.5 CM isolation with chopper differential pair

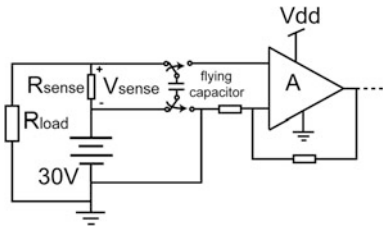

Fig. 1.6 Schematic of CM isolation with the flying capacitor

precision. Finally, the common-mode voltage range (CMVR) of the circuit shown in Fig. 1.5 will not cover both the negative and positive rails [14, 15] (Fig. 1.3).

Another approach to isolate the input CM voltage is to use a so-called flying capacitor [16] to sample and hold the input signal, as shown in Fig. 1.6. The CM voltage at the input of the succeeding amplifier is set by a feedback resistor network and so it can be realized with low-voltage circuitry. However, the kT/C noise associated with the sample-and-hold action of the flying capacitor increases the total input-referred noise. Moreover, continuous-time operation is not possible. Last but not least, the input switches must once more be able to handle the large CM signal.

From the above introduction, it seems that none of these approaches is very satisfactory. Thus, a new approach is required.

1.3 A Promising Solution: Capacitively Coupled Chopper Amplifier

An intuitively appealing solution to the problem of CM isolation is the use of capacitive coupling. Capacitors are widely available in most standard CMOS process and exhibit a natural ability to block DC signals without any extra power consumption. Thus, a capacitively coupled amplifier will perfectly reject DC CM voltages, as long as they are smaller than the breakdown voltage of the coupling capacitors (Fig. 1.7). Although the breakdown voltages of on-chip capacitors is usually less than 100 V, this is still sufficient for many applications. However, it is

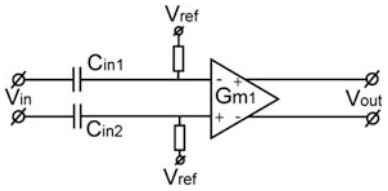

Fig. 1.7 Schematic of a capacitively coupled amplifier

also obvious that the DC input signal is also blocked. One solution is to use the chopping technique described in the previous sections to up-modulate the input signal. This has the added advantage of suppressing the offset and low 1/*f* noise of the input stage.

However, the concept of capacitively coupled chopper amplifiers is not new! As early as 1940, the classic capacitively coupled chopper amplifier shown in Fig. 1.8 was invented [6]. The input signal is up-modulated by the input chopper, amplified, and finally de-modulated by the output chopper. However, the CM voltage is also modulated and so no CM isolation can be obtained. The differential structure, as shown in Fig. 1.9, changes the story completely. The input chopper modulates the DC differential signal to high frequencies, which can then travel through the input capacitors. The DC CM signal, however, is blocked. As a result, the input CM level of the succeeding amplifier can be fixed arbitrarily via biasing resistors $R_{1,2}$ and so the amplifier can be implemented with low-voltage circuitry. At the amplifier's output, an output chopper demodulates the signal back to the base band. The offset and 1/*f* noise of this amplifier, however, are blocked/filtered by the output capacitors. To prevent its output from saturating, the gain of the (transconductance) amplifier is limited by the output resistors $R_{\text{out1,2}}$. However, the amplifier cannot be used as an operational amplifier (opamp) due to its low gain or an instrumentation amplifier (IA) due to its inaccurate gain (G_{m1}*$R_{\text{out1,2}}$).

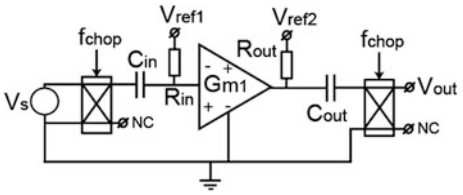

Fig. 1.8 Schematic of a classic single-ended capacitively coupled chopper amplifier

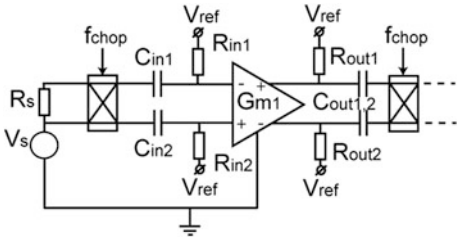

Fig. 1.9 Schematic of a classic fully differential capacitively coupled chopper amplifier

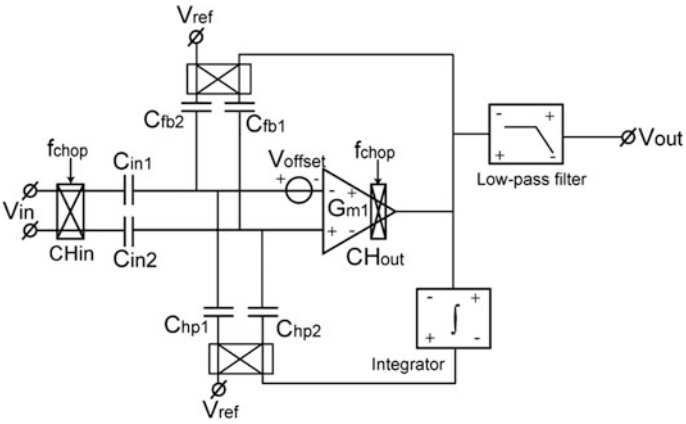

Fig. 1.10 Block diagram of the first CCIA: from Timothy Denison [18]

In 2007, the first capacitively coupled chopper instrumentation amplifier (CCIA) was described by Timothy Denison [17]. It is shown in Fig. 1.10. This work represents a great improvement on Fig. 1.9 topology. By eliminating the need for $R_{out1,2}$ and $C_{out1,2}$, the open-loop gain of the amplifier can be quite large. A chopped capacitor feedback path ensures that the gain of the IA is accurately defined as $C_{in1,2}/C_{fb1,2}$. Since the amplifier was intended for biomedical applications, a DC servo loop was employed (an SC integrator and $C_{hp1,2}$) to give it a high-pass characteristic. The up-modulated offset and $1/f$ noise of G_{m1} was suppressed by a second stage (not shown) which acts as a low-pass filter. Although not designed for high input CM voltages, this CCIA demonstrated the feasibility of realizing on-chip capacitively coupled precision IAs. In this thesis, the design of capacitively coupled chopper IAs and opamps that can handle large input CM voltages, in some cases even larger than their supply voltages, will be explored.

1.4 Challenging Issues

Although the use of capacitively coupled chopper amplifiers seems to be a promising way of obtaining both wide CMVR and high DC precision, there are still many issues to be solved. The first issue is the robust implementation of the input chopper, which must handle the high CM voltage present before the input capacitors. Otherwise, the maximum input CM will be limited by the input chopper and not by the breakdown voltage of the input capacitors.

The input impedance of the amplifier is also an issue. Since the input capacitors are constantly switched between V_{in+} and V_{in-}, they are constantly being charged and discharged, which requires a certain amount of input current. The resulting impedance depends on the input capacitance and the chopping frequency, and

typically ranges from hundreds of kilo-ohms to tens of megaohms, which may not be high enough for some applications. Thus, techniques to boost the input impedance are required.

Since the input DC CM voltage is blocked, the DC CM level of the amplifier's input stage (G_{m1} in Fig. 1.9) must be fixed by something else. This can be done by using biasing resistors ($R_{1,2}$ in Fig. 1.9). However, as will be shown later, these resistors introduce noise, and so must be rather large (hundreds of megaohms). Thus, another challenge is that of realizing such large resistors in an area-efficient and relatively accurate manner.

A fourth issue of capacitively coupled chopper amplifiers is the up-modulated offset and 1/*f* noise of the amplifier. Without the AC-coupling output capacitors shown in Fig. 1.9, the amplifier's offset will be up-modulated by the output chopper and result in ripple. This is usually not acceptable and, thus, must be suppressed effectively. A low-pass filter (Fig. 1.10) is the most straightforward way but it often involves the use of large passive components. In recent years, more effective ripple-reduction techniques [18–21] have been developed. However, care must be taken to minimize the extra area and power required, especially in low power and cost sensitive applications.

Finally, when a ripple-reduction technique is applied, it is very likely to introduce a notch at the chopping frequency in the amplifier's transfer function. This notch limits the amplifier's useable bandwidth and, moreover, results in a step response that will exhibit a certain amount of undesirable ringing. Thus, techniques of dealing with such transfer function notches must be devised.

1.5 Organization

In Chap. 2, the chopping technique, which has been frequently mentioned in the above, is introduced in detail. Several other commonly used dynamic offset cancelation techniques are also introduced. Like chopping, these techniques can also be used to achieve low offset and 1/*f* noise. As mentioned above, the up-modulated offset and 1/*f* noise due to chopping results in ripple, which must be sufficiently suppressed. Thus, ripple-reduction techniques will also be discussed.

In Chap. 3, the proposed capacitively coupled chopper topology for both opamps and IAs will be described. Its operating principles will be discussed in detail as well as its strengths and weaknesses.

As mentioned earlier, input capacitive coupling is not the only prerequisite to obtaining wide input CMVR. Thus, specially designed input choppers with wide CMVR are proposed, which will be presented in Chap. 4.

In Chaps. 5, two opamp prototypes employing the capacitively coupled chopper topology are presented. First, an overview of the state of the art is given. Later, the design considerations of the prototypes on both system level and transistor level are described. A single-path capacitively coupled chopper opamp is presented first, followed by a multipath capacitively coupled chopper opamp that improves the

high-frequency performance and step response of the single-path opamp. Measurement results of each opamp will be given.

In Chaps. 6 and 7, two IA prototypes employing the capacitively coupled chopper topology will be proposed. The first IA features a ±30 V input CMVR and high power efficiency and is designed for HV current-sensing applications. The second IA is wireless sensor node, where power efficiency and small chip area are critical. It can be operated in two modes: a DC mode for DC and low frequency signals sensing; and an AC mode for biomedical signals such as ECG sensing. As in Chap. 5, a state-of-the-art overview will be given at the beginning of each chapter. The systematic and transistor level designs will be presented as well as experimental results.

The thesis ends with conclusions and future work, which are presented in Chap. 8. Two capacitively coupled chopper analog-to-digital converters (ADC) are proposed as future work, which can directly digitize a signal source with high CM voltage. The original contributions of the author are listed at the end of the chapters.

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Chapter 2
The Chopping Technique

As briefly explained in Chap. 1, the chopping technique has been applied to convert DC input signals into AC signals that can then be capacitively coupled to the input stage of a capacitively coupled amplifier. Since chopping up-modulates offset and 1/*f* noise away from DC, high precision, i.e., microvolt offset and low 1/*f* noise, can be achieved. These characteristics make such amplifiers ideally suited for the amplification of small low-frequency signals. In this chapter, the basic working principle of chopping and its application in precision amplifiers will be discussed. It will be shown that chopping usually results in AC ripple at the chopping frequency, which must then be suppressed. Thus, the techniques to reduce this ripple will also be described. After this, the non-idealities of chopping will be discussed, followed by a summary of its pros and cons. Finally, conclusions will be drawn at the end of the chapter.

2.1 Basic Working Principle

Chopping involves the use of two synchronized polarity-reversing choppers [1–4] for precise modulation and demodulation. Each chopper consists of four switches driven by clock signals with two complementary phases at a certain chopping frequency (f_{chop}). In CMOS technology, the switches can be simply implemented by MOSFETs, as shown in Fig. 2.1. In the time domain, as shown in Fig. 2.2, the input chopper converts an input DC signal into a square wave. After amplification, the output chopper demodulates this square wave back to DC. In the frequency domain, the input chopper moves the DC signal to the odd harmonics of f_{chop}, and the output chopper moves the high-frequency components back to DC.

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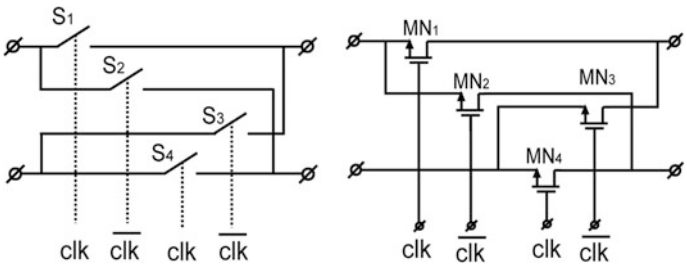

Fig. 2.1 Schematic of a chopper and its implementation with NMOS transistors

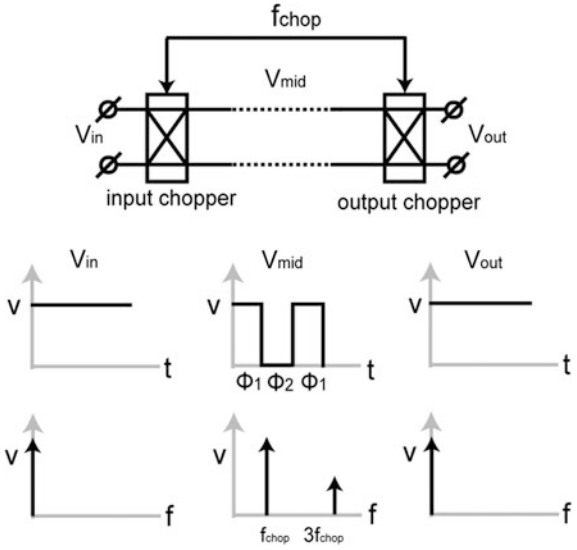

Fig. 2.2 Working principle of two synchronized choppers

2.2 Basic Chopper Amplifier Topologies

2.2.1 Basic Chopper Opamp and Instrumentation Amplifier Topologies

When chopping is applied to an opamp, as shown in Fig. 2.3, the input signal is first moved to the odd harmonics of f_{chop} by CH_{in}, then amplified, and finally moved back to DC. Meanwhile, the offset and $1/f$ noise of G_{m1} are up-modulated by CH_{out} to the odd harmonics of f_{chop}. Thus, ideally, an offset- and $1/f$ noise-free opamp is obtained. It is worth pointing out that in Fig. 2.3, the effective DC gain of the opamp is equal to the gain of G_{m1} at f_{chop}, which is usually much lower than its gain at DC. Thus, to ensure sufficient gain, multiple gain stages are often employed [5]. In a two-stage opamp, for instance, the output chopper (CH_{out}) can be located at the

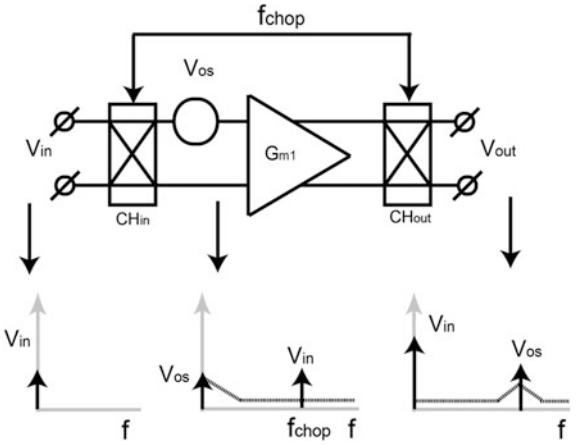

Fig. 2.3 Voltages in the frequency domain in a chopper amplifier

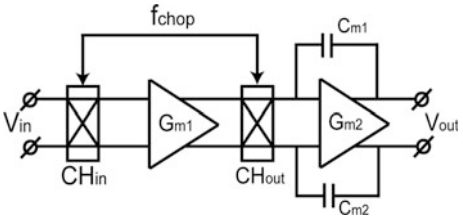

Fig. 2.4 Schematic of a two-stage chopper opamp

input of the second stage, as shown in Fig. 2.4. The amplifier's effective DC gain is then the gain of G_{m1} at f_{chop} multiplied by the DC gain of G_{m2}.

Chopping usually does not introduce extra noise, especially when the choppers are positioned at low impedance nodes. In the situation of Fig. 2.4, for instance, the main noise source is the on-resistance of the input chopper. Thus, by making this low enough, its noise contribution can be made negligible.

To realize a chopper instrumentation amplifier (IA), a resistive feedback network can be added around a chopper opamp (Fig. 2.5). If high-input impedance is

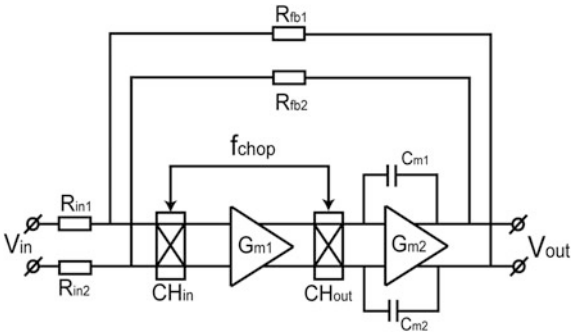

Fig. 2.5 Schematic of chopper IA with resistive feedback network

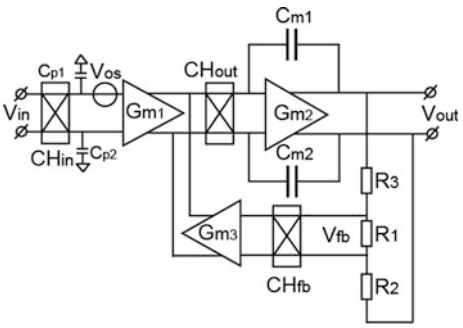

Fig. 2.6 Schematic of a chopper current feedback IA

required, an extra feedback transconductance G_{m3} can be employed together with a resistive divider (Fig. 2.6). The latter topology is known as an indirect current feedback IA (CFIA) [1, 3]. The high-open-loop gain of the opamp ensures that the output current of G_{m1} cancels that of G_{m3}, so that V_{in} is equal to V_{fb}. Thus, V_{out} will be equal to $V_{in} \times \frac{G_{m1}}{G_{m3}} \times \frac{R_1+R_2+R_3}{R_1}$. In this case, G_{m3} also introduces offset and $1/f$ noise; thus, a third chopper CH_{fb} must be employed.

The up-modulated offset and $1/f$ noise in both chopper opamps and IAs, however, will appear as output ripple which must then be eliminated. A straightforward way of doing this is by employing a low-pass filter at the output of the amplifier. However, the filter itself can introduce extra offset (in the case of an active filter) and noise (both for active and for passive filters), which are only suppressed by the closed-loop gain of the previous chopper amplifier and, thus, may not be sufficiently reduced [6]. Moreover, to obtain sufficient filtering, the cutoff frequency of the filter should be sufficiently low, which also limits the bandwidth of the whole signal path (chopper amplifier + filter). Thus, alternative ripple-reduction techniques are required.

The chopper stabilization technique is one way to suppress chopper ripple while not necessarily introducing extra offset and $1/f$ noise, and affecting the signal bandwidth. It involves placing a chopper amplifier in an auxiliary signal path, which then does not limit the bandwidth of a main amplifier. By limiting the bandwidth of the auxiliary single path, its ripple is reduced. In the following, the chopper stabilization technique will be discussed in more detail.

2.2.2 *Chopper Stabilization*

The basic topology of a chopper-stabilized amplifier is shown in Fig. 2.7 [1, 3, 7]. The amplifier consists of two signal paths: a main signal path consisting of A_1 and an auxiliary signal path consisting of A_2 and A_3. This topology has been used in several state-of-the-art designs [7–10]. The main signal path provides wide signal

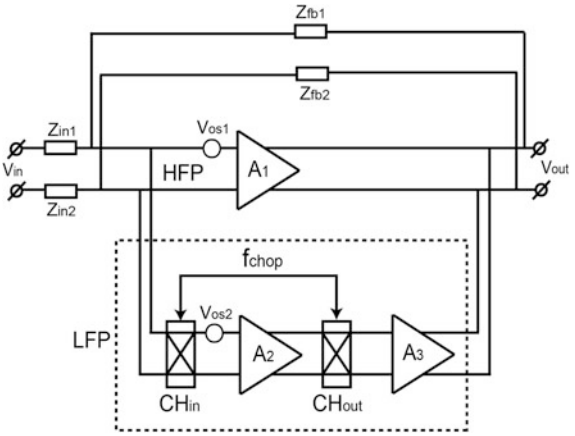

Fig. 2.7 Block diagram of a chopper-stabilized amplifier with negative feedback network

bandwidth and is thus often referred to as the high-frequency path (HFP), while the auxiliary path provides low offset and high DC gain, usually has limited bandwidth, and thus is often called as the low-frequency path (LFP). To achieve low offset, the offset of the HFP must be taken care of. In the presence of a global negative feedback as shown in Fig. 2.7, the offset of A_1 (V_{os1}) will be amplified and then fed back to the input of the LFP. Thus, it will be corrected by the high-gain LFP. The residual offset due to V_{os1} can be expressed as [3]:

$$V_{error} = \frac{V_{os1} \times A_1}{A_2 \times A_3}. \tag{2.1}$$

Thus, as long as there is sufficient gain in the LFP, the residual offset is negligible. It is worth mentioning that the low-frequency $1/f$ noise of the HFP is also suppressed by the LFP in the same manner. The offset of the LFP, however, is removed by chopping.

The main advantage of chopper stabilization is that it can achieve high bandwidth and high DC accuracy at the same time. The chopping ripple generated in the LFP is suppressed by limiting its bandwidth, e.g., by the deliberate insertion of a low-pass filter (often an integrator). The disadvantage of this approach, however, is the reduction in power efficiency associated with the use of two signal paths. Another potential concern is that when microvolt-level residual ripple is required, a low-pass filter requiring large passive components may be needed to restrict the bandwidth of the LFP. This can increase the chip area significantly. Thus, better methods to sufficiently reduce the chopping ripple without consuming too much power and chip area are required.

2.3 Ripple-Reduction Techniques

Consider the case of the CFIA shown in Fig. 2.6, and if its bandwidth is lower than the chopping frequency, then the ripple voltage V_{ripple} at its output will be a triangular wave and its amplitude can be estimated by:

$$V_{\text{ripple}} = \frac{V_{\text{os}} \times G_{\text{m1}}}{2 \times f_{\text{chop}} \times C_{\text{m1,2}}}, \tag{2.2}$$

where V_{os} is the offset of G_{m1}. For instance, with V_{os} = 5 mV, G_{m1} = 100 μS, $C_{\text{m1,2}}$ = 10 pF, and f_{chop} = 50 kHz, V_{ripple} is 0.5 V. Such a large ripple is usually not tolerable and must be removed. To suppress a 0.5 V ripple to, for instance, 50 μV, a suppression factor of 10,000 is needed. This cannot be easily achieved by either employing a low-pass filter at the output of the amplifier or chopper stabilization.

Recently, many highly effective ripple-reduction techniques have been published [4, 5, 7–15]. Four of these will be discussed here; they are as follows: a switched-capacitor (SC) notch filter [7, 8]; an AC-coupled ripple-reduction loop (RRL) [11]; an auto-correction loop [10]; a digitally assist RRL [12]; and the combination of chopping and auto-zeroing [16, 17]. These techniques will be discussed in the following sections.

2.3.1 *The Switched-capacitor (SC) Notch Filter*

A simplified SC notch filter published by Burt [8] is shown in Fig. 2.8, along with its timing diagram. An SC network is placed at the output of CH_{out}. The switching frequency f_s is chosen to be the same as f_{chop}, but with a 90° phase shift (Fig. 2.8).

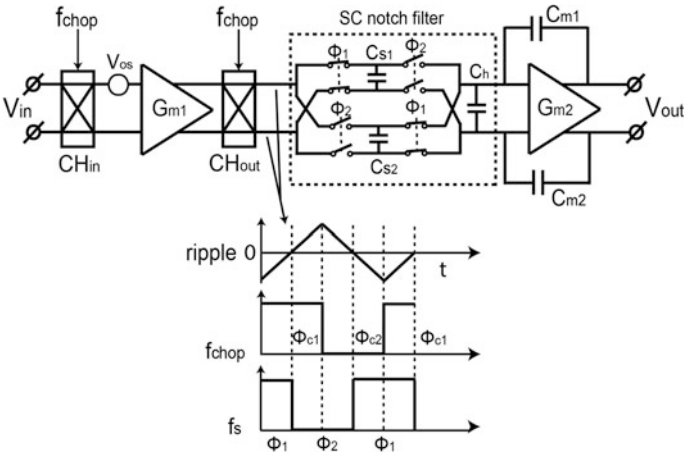

Fig. 2.8 Simplified block diagram of an amplifier employing the SC notch filter

During the first half of the chopping phase Φ_{c1}, the ripple is sampled on C_{s1}. Assuming that the ripple has a triangular shape, its amplitude will be ideally zero on the falling edge of the sampling clock f_s. At this moment, C_{s1} is disconnected from the output of CH_{out} and then connected to G_{m2} until the rising edge of f_s. In this way, the ripple is not seen by G_{m2}. To obtain a quasi-continuous signal, a second sampling capacitor C_{s2}, operated in anti-phase, replicates the operation of C_{s1}. In the frequency domain, the SC network forms a narrow notch around f_{chop} in the transfer function of the amplifier. This filters out the ripple while leaving the low-frequency signal untouched. The noise introduced by the SC notch filter is mainly kT/C noise. However, since the notch filter is behind the first stage, its noise should be sufficiently suppressed by the gain of the first stage especially in the low-frequency range.

This approach is highly power efficient, since the SC network does not consume any bias current. Moreover, since it operates continuously, it is ideally immune to offset drift. However, it also has a few drawbacks. One drawback is the phase delay of the SC notch filter, which is 90° at f_{chop}. Thus, it will cause instability around f_{chop}, assuming the amplifier's bandwidth is higher than f_{chop}. As a result, a chopper stabilization architecture (Fig. 2.7) is employed by [8] and the SC notch filter is used in the LFP. In this way, the high-frequency behavior is mostly taken over by the HFP, which does not suffer from this delay. Secondly, this approach can potentially consume a large chip area. This is because a ripple voltage is integrated on $C_{s1,2}$, whose peak amplitude should be kept within the output swing of G_{m1}. For instance, with 10 mV V_{os}, 100 μS G_{m1}, and 10 kHz f_{chop}, the value of $C_{s1,2}$ required to limit the peak ripple voltage V_{ripple} within 2.5 V is:

$$C_{s1,2} = \frac{V_{off} \times G_{m1}}{2 \times f_{chop} \times V_{ripple}} = \frac{1\ \mu}{2 \times 10\ \text{k} \times 2.5} = 20\ \text{pF} \tag{2.3}$$

The situation becomes more severe in low noise and low voltage designs, where G_{m1} must be increased and its output swing will be restricted. Increasing f_{chop} can help save chip area. However, it also results in more charge injection and clock feed-through errors, which will be explained later in Sect. 2.4.

2.3.2 AC-Coupled Ripple-Reduction Loop

In 2009, an AC-coupled ripple-reduction loop (RRL) was described by Wu [12]. A simplified block diagram of the RRL is shown in Fig. 2.9. It consists of two sensing capacitors $C_{s1,2}$, a demodulation chopper CH_{RRL}, an integrator built around G_{m3}, and a compensation transconductor G_{m4}. $C_{s1,2}$ sense the ripple and convert it into an AC current. Assuming the ripple is a triangular wave, the AC current is then a square wave as shown in Fig. 2.9. The AC current is then demodulated to DC by

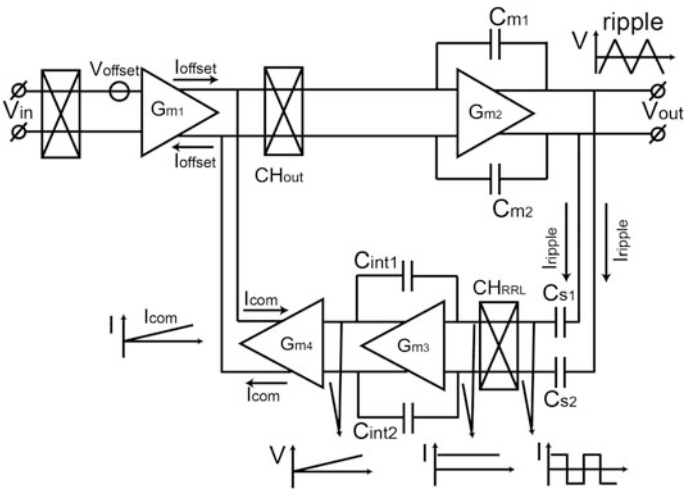

Fig. 2.9 Block diagram of the AC-coupled ripple-reduction loop

CH_{RRL} and integrated by the integrator built around G_{m3}. The output DC voltage of the integrator is then converted into a compensation current I_{com} by G_{m4}, which cancels the offset current I_{offset} of G_{m1}. When I_{com} is equal to I_{offset}, the ripple will completely disappear.

Like the SC notch filter, the RRL creates a notch at f_{chop}. The effectiveness of the RRL greatly depends on its loop gain, which in turn depends on the design parameters such as the DC gain of G_{m3}. The width of the notch can be designed by adjusting parameters such as G_{m4}, $C_{int1,2}$, and $C_{m1,2}$. A complete theoretical analysis, including the calculation of the notch width, can be found in [12].

The noise of the RRL is injected into the amplifier via G_{m4}. To minimize its contribution, G_{m4} is often designed to be much smaller than G_{m1}. However, the tail current of G_{m4} must then be sufficient to compensate for the maximum I_{offset}. Thus, G_{m4} is often biased in strong inversion or with resistor degeneration.

A problem of the circuit shown in Fig. 2.9 is the offset of the integrator built around G_{m3}. This offset will be up-modulated by CH_{RRL} and directly coupled to the output of the amplifier via $C_{s1,2}$. Thus, in reality, the circuit shown in Fig. 2.9 is hardly employed. To correct this error, the offset of G_{m3} must be removed. The methods of doing so will be introduced in Chaps. 5, 6, and 7.

The RRL is not as power efficient as the SC notch filter. However, it offers more design flexibility. The width of the notch, thus the phase delay, for instance, can be designed by adjusting several parameters such as f_{chop}, G_{m4}, $C_{int1,2}$, and $C_{m1,2}$ [12]. Moreover, it is not located in the main signal path, which makes the frequency compensation more relaxed when compared to the SC notch filter.

2.3.3 Auto-Correction Feedback Loop

This technique was first described by Kusuda [11] in 2010. A simplified block diagram is shown in Fig. 2.10. Unlike the AC-coupled RRL, the auto-correction feedback loop senses the ripple at the output of CH_{out}. In this case, a small square-wave ripple is present at the output of CH_{out}. This small ripple voltage is then sensed and converted into a current by G_{m3} and demodulated to DC by CH_{RRL}. This current is then integrated by the integrator built around G_{m4}, which is further converted into a compensating current I_{com} by G_{m5}.

However, not only the ripple but also some of the input signal will be sensed and suppressed by this loop. For instance, in the presence of a DC input signal, a DC signal voltage will appear at the input of G_{m3}, which will then be up-modulated and filtered by the integrator built around G_{m4}. A residual AC signal voltage will then be converted to an AC current by G_{m5}, which will compensate the AC signal current of G_{m1}. This can result in a significant gain reduction in the signal band. To solve this problem, a notch filter is employed which removes the up-modulated residual signal voltage at the output of G_{m4}. In this way, the DC signal is ideally not affected by the auto-correction loop.

Similar to the AC-coupled RRL, the noise of the auto-correction loop is injected into the main signal path via G_{m5}. Thus, to limit this noise, G_{m5} should be much smaller than G_{m1}.

The power efficiency of the auto-correction loop is comparable to that of the AC-coupled RRL. Sufficient ripple suppression can be guaranteed by increasing the loop gain, which in turn depends on the parameters such as the DC gain of G_{m4}.

The advantage of the auto-correction loop compared to the AC-coupled RRL shown in Fig. 2.9 is that it does not sense at the output of the amplifier. This is

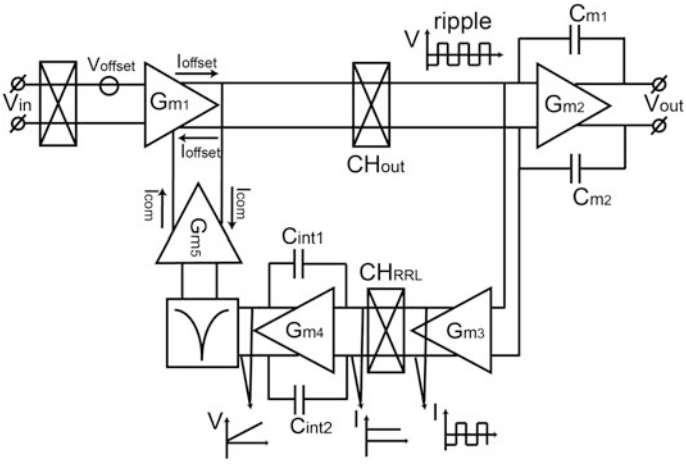

Fig. 2.10 Simplified block diagram of an auto-correction loop

desired in applications where the amplifier is succeeded by a circuit that generates extra ripple at the output, such as the charge injection and clock feed-through of the input switches of a SC circuit. This extra ripple may overload the AC-coupled RRL and thus ruin its performance. The disadvantage of this approach, however, is also due to its sensing point, which is at the virtual ground instead of the amplifier's output. This means that the ripple signal is often quite small and thus a more accurate RRL with higher loop gain is required. The need for a notch filter also increases the complexity of this approach.

2.3.4 Digitally Assisted Trimming

This technique was described by Xu [13] in 2011. A simplified block diagram of this approach is shown in Fig. 2.11. After start-up, the amplifier's input is shorted, and thus, its offset voltage will be converted into an offset current I_{os} by G_{m1} and appears as a ripple at the output. The peak voltage of this ripple is sampled by a sample-and-hold (S&H) circuit and then converted into digital bits by an ADC. The digital bits are then converted into a current by a DAC, compensating I_{os}. Later, when the RRL is settled, the digital bits will be frozen and the amplifier will be connected to the signal source.

The RRL will be shut down after it settles; thus, this approach is very power efficient. The main disadvantage of this approach is that it is vulnerable to offset drift after the RRL is frozen. Moreover, to correct the offset sufficiently, high resolution is required for both ADC and DAC, which can be tricky to implement. Reducing the resolution of the ADC/DAC will thus result in residual ripple [13].

2.3.5 Chopping + Auto-Zeroing

Before explaining the technique of combining chopping and auto-zeroing, an introduction of auto-zeroing is necessary, which will be given in the following.

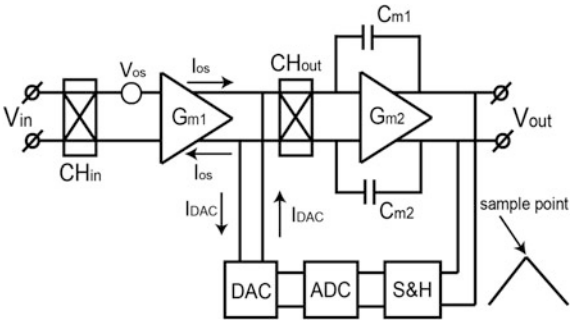

Fig. 2.11 Digitally assisted RRL

2.3.5.1 The Auto-Zeroing Principle

Auto-zeroing is also a commonly used technique to achieve low offset [1–3]. The basic principle of auto-zeroing is illustrated in Fig. 2.12. A SC network driven by a digital clock is built around an opamp G_{m1}. In the first clock phase Φ_1, G_{m1} is connected in unity-gain configuration, and its offset is thus sampled on C_{az2} and meanwhile appears at its output. In the next clock phase Φ_2, G_{m1} amplifies the input signal, and its offset V_{os} is canceled by the voltage stored on C_{az2} in Φ_1. Ideally, the voltage stored on C_{az2} should be equal to V_{os}, and thus, G_{m1} appears to be offset free. Similarly, the low-frequency $1/f$ noise components are also stored on $C_{az1,2}$ and so are canceled. However, the higher frequency $1/f$ noise components are less correlated and so cannot be effectively canceled [2].

Auto-zeroing can also be applied in an auxiliary amplifier. This is shown in Fig. 2.13 [1, 2], where an offset compensation loop is implemented around the

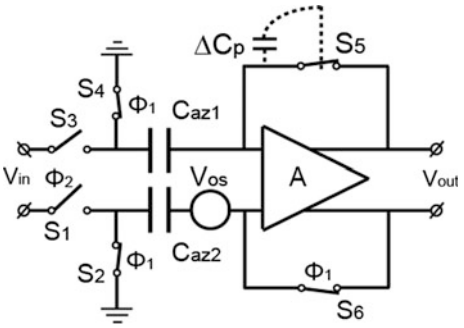

Fig. 2.12 Basic block diagram of a simplified auto-zeroed amplifier

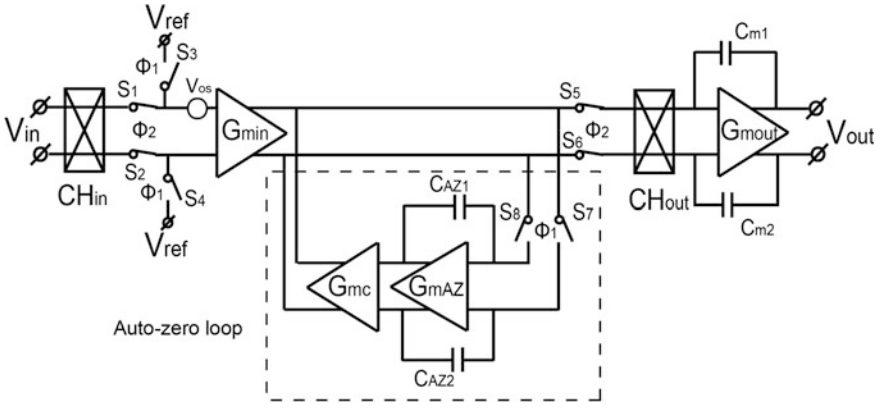

Fig. 2.13 Block diagram of an amplifier using auto-zeroing auxiliary loop

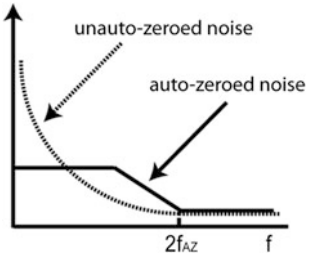

Fig. 2.14 Noise folding caused by auto-zeroing

input transconductor G_{min}. In Φ_1, G_{min} is disconnected from the signal source. Its input is shorted so that its offset voltage is converted into an offset current and then integrated on the integrator built around G_{mAZ}. The output voltage of G_{mAZ} is then converted into a current by G_{mc}, which will cancel the offset current of G_{min} completely. In Φ_2, G_{min} is connected to the input signal, and the input of G_{mAZ} is disconnected from the output of G_{min}. The integrator built around G_{mAZ}, however, holds the compensation voltage stored in Φ_2, so that the offset of G_{min} is also compensated in Φ_2. The advantage of using an auto-zeroing loop rather than its simplified counterpart (Fig. 2.13) is that the errors of auto-zeroing (such as the charge injection and clock feed-through errors of $S_{5,8}$ in Fig. 2.13) are better suppressed by its high loop gain. Thus, the auto-zeroing loop is more accurate. Since there is nothing up-modulated, no ripple is expected ideally.

However, auto-zeroing has a major drawback: increased baseband noise. The sample-and-hold (S&H) action of $C_{az1,2}$ in Fig. 2.12 will result in noise folding, which increases the noise level at low frequencies [1–3]. This effect is illustrated in Fig. 2.14. It can be seen that without auto-zeroing, the low-frequency noise is dominated by the $1/f$ noise, while with auto-zeroing, the low-frequency noise is dominated by the white noise that has been folded back from high frequencies. For the complete (and rather complicated) theory of noise folding, readers are suggested to refer to [2, 18]. For amplifiers employing auto-zeroing loop shown in Fig. 2.13, however, the increased low-frequency noise can have a much smaller bandwidth by reducing the bandwidth of the auto-zeroing loop as explained in [16]. The price, however, is that the auto-zeroing loop will require a longer time to settle.

2.3.5.2 Chopping + Auto-Zeroing

From the above introduction, it is clear that auto-zeroing ideally does not introduce a ripple, but suffers from increased baseband noise. When auto-zeroing is combined with chopping, however, the increased baseband noise can be up-modulated to high frequencies. Thus, a low baseband noise floor can be obtained. This is shown in Fig. 2.15 [17] and Fig. 2.16 [16]. In [17], the increased baseband noise bandwidth is about 2× auto-zeroing frequency. Thus, the chopping frequency is chosen to be 2× auto-zeroing frequency. As a result, low noise is obtained in low frequencies. In [16], however, the auto-zeroing noise bandwidth is reduced by a slow auto-zeroing

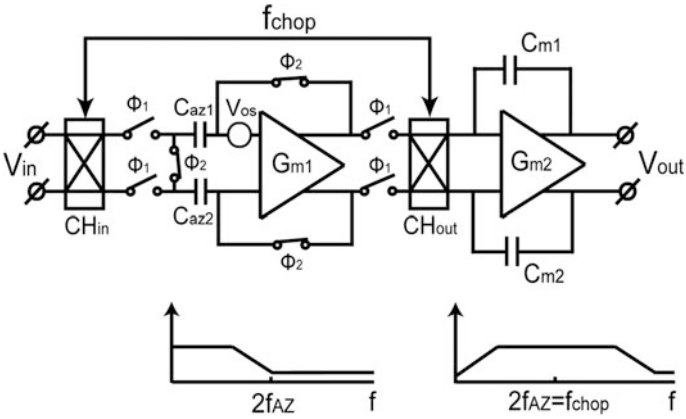

Fig. 2.15 Block diagram of a two-stage amplifier applying both chopping and auto-zeroing

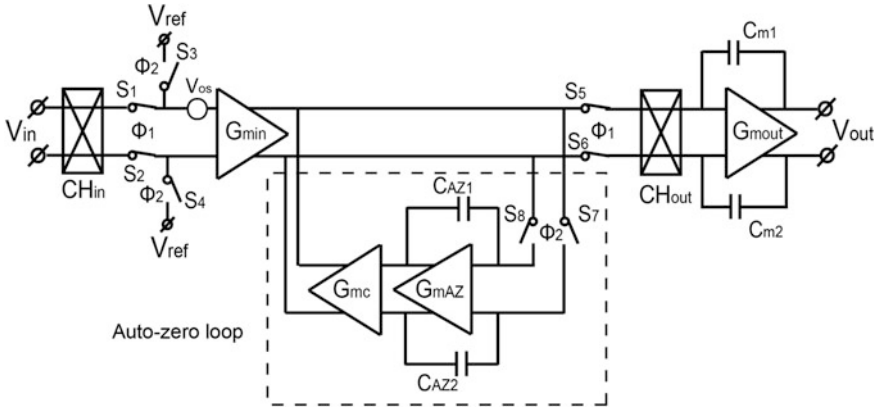

Fig. 2.16 Block diagram of an amplifier employing both chopping and auto-zero

loop. Thus, a lower chopping frequency is chosen, which results in less charge injection and clock feed-through errors.

The advantage of combing chopping and auto-zeroing is that ideally no ripple is expected and a low baseband noise can be obtained. The drawback, however, is that it does not provide continuous-time operation. To obtain continuous-time operation, a ping-pong technique should be employed [19], which involves the use of two identical input stages. During half of the auto-zeroing cycle, one input stage is being auto-zeroed, while the other is amplifying the signal. This approach, however, significantly increases the power consumption of the whole amplifier and thus is less preferred.

2.3.5.3 Summary

The presented ripple-reduction techniques all have their own advantages and disadvantages. The SC notch filter and the digitally assisted RRL are both very power efficient. However, the former suffers from a fixed phase delay and a trade-off between chopping frequency and chip area, while the latter suffers from offset drift and an accuracy compromised by the limited resolutions of the ADC/DAC. The AC-coupled RRL and the auto-correction feedback loop are less power efficient, but offer more design flexibility. Last but not least, chopping combined with auto-zeroing has a trade-off between continuous-time operation and power efficiency.

Apart from the digitally assisted RRL, the SC notch filter, the AC-coupled RRL, the auto-correction loop, and chopping combined with auto-zeroing are immune to offset drift. The basic concept shared by the SC notch filter, the AC-coupled RRL, and the auto-correction loop is the implementation of a notch filter. Thus, when they are applied in a single-path amplifier, they all create a notch in the amplifier's transfer function. And like any type of notch filter, this will result in a ringing step response (Fig. 2.17). The settling time of the ringing is determined by the relative position of the poles and zeros of the notch filter, as explained in [20]. This is undesirable in applications where fast settling is required. Thus, better techniques are required. Although chopping combined with auto-zeroing does not introduce such as notch, its power efficiency is low when continuous-time operation is required.

One solution to suppress a notch in the transfer function is to use chopper stabilization, where the HFP can be used to compensate for the loss of the gain associated with the notch. Design examples will be presented later in Chap. 5.

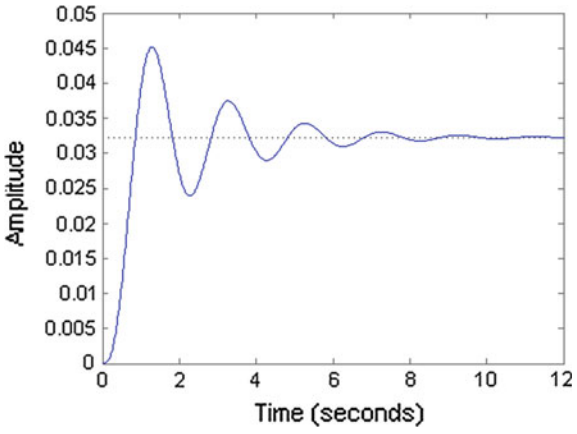

Fig. 2.17 Step response of a notch filter

2.4 Chopping Non-idealities

Regardless of the topology employed, the chopper switches' non-idealities themselves can cause extra offset and ripple. In this section, these non-idealities will be described in detail.

First, a mismatched parasitic capacitance ΔC_{po1} (Fig. 2.18) from the clock line to one of the inputs of CH_{out} results in an AC current. This current can be modeled as an AC voltage at the input of G_{m1}, which, in turn, can be modeled as a residual offset V_{off1} at the input of CH_{in}. This can be roughly estimated as [3]:

$$V_{off1} = \frac{V_{clk} \times \Delta C_{po1} \times 2f_{chop}}{G_{m1}}. \tag{2.4}$$

For instance, with V_{clk} = 3 V, ΔC_{po1} = 1 fF, f_{chop} = 30 kHz, and G_{m1} = 100 μS, V_{off1} is then 1.8 mV. Similarly, a mismatched parasitic capacitance ΔC_{pi1} from the clock line to one of the outputs of CH_{in} again results in an AC current, which is then demodulated by CH_{in} and converted into a voltage by the source resistance R_s. Thus, a second residual input offset V_{off2} is obtained, which can be estimated by Witte et al. [3]:

$$V_{off2} = \frac{V_{clk} \times \Delta C_{pi1} \times 2f_{chop}}{R_{on}}. \tag{2.5}$$

Furthermore, a mismatched parasitic capacitance ΔC_{po2} (Fig. 2.18) introduces an AC clock feed-through spike, which is then filtered by the integrator built around G_{m2} and appears as an output ripple. The amplitude of this ripple V_{rip1} can be estimated by:

$$V_{rip1} = \frac{V_{clk} \times \Delta C_{po2}}{C_{m1.2}}. \tag{2.6}$$

Thus, a residual ripple is obtained. Similarly, the mismatched parasitic capacitance ΔC_{pi2} again introduces an AC clock feed-through current spike at the input of the amplifier, which is then converted into a voltage by the source impedance R_s,

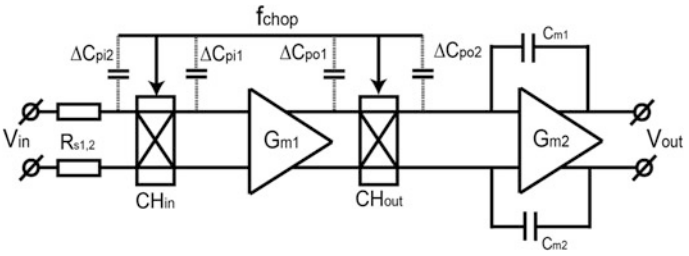

Fig. 2.18 Chopper opamp with mismatched parasitic capacitors

and then filtered by the whole amplifier and appears as another ripple V_{rip2} at the output:

$$V_{rip2} = \frac{V_{clk} \times \Delta C_{pi2} \times R_s \times G_{m1}}{C_{m1.2}}. \tag{2.7}$$

Finally, the mismatch between the chopper switches will result in mismatched charge injection errors, which have the same effects as mismatched clock feed-through as explained above. Thus, to ensure low residual errors, the layout of the choppers, including the chopper switches and the clock lines, must be as symmetrical as possible.

2.5 Chopping Pros and Cons

Chopping ensures continuous-time operation and does not necessarily introduce significant noise as explained before. However, the up-modulated offset and 1/*f* noise will produce a ripple at the output of an amplifier. Thus, ripple-reduction techniques introduced earlier should be employed. Moreover, in ultra-low noise applications, the noise of the on-resistor of the input chopper switches may not be negligible (1 kΩ $\sim$ 4nV/$\sqrt{\text{Hz}}$). To reduce this on-resistance, the overdrive voltage of the chopper switches or the width of the switches should be increased, which can result in more charge injection and clock feed-through errors. Last but not least, chopping can reduce the input impedance of the amplifier as shown in Fig. 2.6. In the presence of both CH_{in} and parasitic capacitors $C_{p1,2}$ at the input of G_{m1} (for instance, gate capacitance of the input pair, parasitic capacitance due to routing), a SC resistor is formed. Its DC differential resistance R_{in} can be calculated by:

$$R_{in} = \frac{1}{f_{chop} \times C_{p1,2}}. \tag{2.8}$$

As a result, compared to a non-chopped amplifier, a chopped amplifier's DC input impedance is lowered. To obtain a higher input impedance, lower chopping frequency and smaller $C_{p1,2}$ should be realized.

2.6 Conclusions

Based on the above, it can be concluded that by employing chopping, capacitively coupled chopper amplifiers can easily obtain low offset and low 1/*f* noise. The ripple due to chopping can also be sufficiently reduced by various ripple-reduction techniques. Building on this introduction to chopping, the working principles of capacitively coupled chopper amplifiers will be discussed in detail in Chap. 3.

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Chapter 3
Capacitively Coupled Chopper Amplifiers

As discussed in Chap. 1, capacitively coupled chopper amplifiers can potentially handle input common-mode voltages far beyond their own supplies. Furthermore, their inherent use of chopping means that they can also achieve microvolt offset and low 1/*f* noise. In this chapter, the operation of capacitively coupled chopper amplifiers will be described in more detail. The capacitively coupled chopper opamp (CCOPA) topology will be presented first (Sect. 3.1), followed by the capacitively coupled chopper IA (CCIA) topology (Sect. 3.2). For both topologies, an analysis will be made of their offset, input-referred noise, and power efficiency and also discussed will be their common-mode rejection ratio (CMRR), input CM voltage range (CMVR), input impedance, and settling and transient issues. For the CCIA especially, an analysis of gain accuracy and output transient will be added. Finally, the chapter ends with conclusions.

3.1 Capacitively Coupled Chopper Opamps (CCOPA)

A capacitively coupled chopper opamp (CCOPA) is shown in Fig. 3.1. It consists of two gain stages G_{m1} and G_{m2}, a couple of choppers CH_{in} and CH_{out}, two input capacitors $C_{in1,2}$ and two biasing resistors R_{b1} and R_{b2}. The DC signal is first up-modulated by CH_{in}, travels to the input of G_{m1} through $C_{in1,2}$, and is then converted into an AC current. The AC current at the output of G_{m1} is demodulated by CH_{out} and integrated on the integrator built around G_{m2}.

Unlike the conventional chopper opamps shown in Figs. 2.3 and 2.4, whose input transconductors are usually variations on a differential pair, the input transconductor of the CCOPA shown in Fig. 3.1 consists of the combination of $C_{in1,2}$, $R_{b1,2}$ and G_{m1}. This has consequences for its input characteristics. The equivalent input transconductance G_{min} can be expressed as follows:

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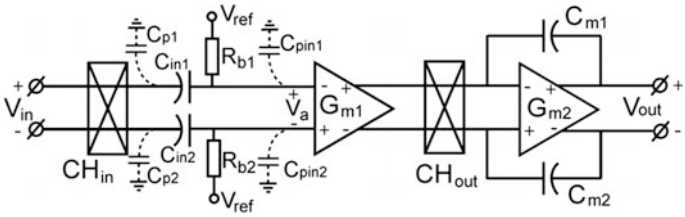

Fig. 3.1 A block diagram of a capacitively coupled operational amplifier

$$G_{\min} = G_{m1} \frac{j\omega R_{b1,2} C_{in1,2}}{1 + j\omega R_{b1,2} C_{in1,2}} \tag{3.1}$$

It is obvious that $G_{\min}$ has a high-pass transfer function, with a corner frequency at $1/2\pi R_{b1,2} C_{in1,2}$ Hz. Since the input stage is chopped, it handles signals at the chopping frequency f_{chop}. And so the high-pass corner of $G_{\min}$ should be designed well below f_{chop}, so that the effective input transconductance will be roughly equal to G_{m1}.

3.1.1 Offset and 1/f Noise

As explained in Chap. 2, the offset and 1/*f* noise of G_{m1} are up-modulated by CH_{out}, filtered by the integrator built around G_{m2}, and finally appear as ripple at the output of the amplifier. This ripple can be suppressed by the ripple-reduction techniques introduced in Chap. 2. Due to the use of chopping, the CCOPA can obtain low offset and 1/*f* noise.

3.1.2 Noise and Power Efficiency

To achieve high power efficiency, G_{m1} is usually biased in weak inversion. However, the presence of parasitic capacitances $C_{pin1,2}$ at the input of G_{m1}, e.g., the bottom-plate parasitic capacitances of $C_{in1,2}$, layout parasitics, and the input capacitance of G_{m1} (Fig. 3.1), means that Eq. (3.1) must be modified as follows:

$$G_{\min} = G_{m1} \frac{j\omega R_{b1,2} C_{in1,2}}{1 + j\omega R_{b1,2} \left(C_{in1,2} + C_{pin1,2}\right)} \tag{3.2}$$

It can be seen that the high-pass corner of $G_{\min}$ decreases slightly to $1/2\pi R_{b1,2}\left(C_{in1,2} + C_{pin1,2}\right)$. But more importantly, at f_{chop}, $G_{\min}$ decreases by a factor equal to $C_{in1,2}/\left(C_{in1,2} + C_{pin1,2}\right)$. In consequence, the voltage noise of G_{m1} will be amplified by $\left(C_{in1,2} + C_{pin1,2}\right)/C_{in1,2}$ when referred to the input of $G_{\min}$. Thus, to minimize noise, $C_{pin1,2}$ must be designed to be much smaller than $C_{in1,2}$.

Apart from G_{m1}, each biasing resistor $R_{b1/2}$ also generates thermal noise, whose input-referred value can be expressed as follows:

$$V_{nRb} = \frac{1}{2\pi \times C_{in1,2} \times f_{chop}} \sqrt{\frac{4\ kT}{R_{b1,2}}} \tag{3.3}$$

For good power efficiency, this noise source should be much smaller than the noise contributed by G_{m1}. Thus, the resistance of $R_{b1,2}$ is normally very high (tens of Mega ohm). Different implementing ways of these resistors in a compact manner will be described in Chaps. 5, 6, and 7.

A common misunderstanding about a capacitively coupled chopper amplifier is that it suffers from the same noise-folding problems as an amplifier with a sample-and-hold (S&H) circuit at its input, e.g., one using the flying capacitor technique presented in Chap. 1 [1]. In the latter case, large capacitors may be required to achieve low noise [2]. However, a capacitively coupled chopper amplifier does not suffer from the same noise-folding problem. This is because the input capacitors $C_{in1,2}$ (Fig. 3.1) are always connected to the input source, and thus, no S&H action is involved. As a result, the noise voltage contributed by the input capacitors and chopper is equal to the noise voltage of the chopper's on-resistance, which is in most cases negligible.

3.1.3 Common-mode Rejection Ratio (CMRR) and Common-mode Voltage Range (CMVR)

The DC CMRR of a CCOPA should be quite high. Assuming that the CMRR of CH_{in} is infinite, then any DC CM input voltage will be completely blocked by $C_{in1,2}$, and so no errors can be created.

With a properly designed input chopper CH_{in}, the input CMVR of the CCOPA can be potentially increased to the breakdown voltage of the input capacitors $C_{in1,2}$. And very importantly, this does not cost any extra power. The input CM voltage of G_{m1} is set to an arbitrarily low reference voltage via $R_{b1,2}$, and thus, it can employ a simple low-voltage PMOS/NMOS differential pair. This is a big advantage of a CCOPA compared to other conventional high-voltage opamps, which must employ high supply voltages to expand their CMVR [3–5], and thus, consume more power.

3.1.4 Input Impedance

The input impedance of the CCOPA is relatively low, since $C_{in1,2}$ are switched between V_{in+} and V_{in-} in every clock cycle. This requires charging and discharging

current from the signal source. Thus, the input chopper and capacitors circuit can be seen as a resistor connected between V_{in+} and V_{in-} terminals. The value of this resistance can be calculated as follows:

$$Z_{in} = \frac{1}{2f_{chop}\left(C_{pin1,2} + C_{p1,2}\right)} \tag{3.4}$$

In an opamp, however, this is not critical because in the presence of an external feedback network, the CCOPA's high open-loop gain will make its input a good virtual ground, at which the signal swing is nearly zero. Thus, a relatively low input impedance is tolerable.

3.1.5 Settling and Transient Issues

A disadvantage of a CCOPA is that the speed of its CM response is limited by the time constant formed by $C_{in1,2}$ and $R_{b1,2}$ as follows:

$$\tau = R_{b1,2} \times C_{in1,2} \tag{3.5}$$

When the CM input signal is a step function, a transient current will be injected into $R_{b1,2}$ via $C_{in1,2}$, and consequently, the voltage at the input of G_{m1} will rapidly increase or decrease. Protection diodes should then be added in parallel to $R_{b1,2}$ to limit the maximum CM voltage to $V_{ref} \pm 0.7$ V at the input of G_{m1}. For this voltage to come back to 0.99 V_{ref}, a time equal to at least 5τ ($\tau = R_{b1,2} \times C_{in1,2}$) is then needed. During this time, any mismatch between R_{b1} and R_{b2} will result in a temporary offset voltage at the input of G_{m1}, which will in turn generate output ripple. When ripple-reduction techniques (Sect. 2.3) are employed, this temporary offset can be suppressed.

Another situation is that when a continuous CM sine wave with an amplitude of A_{sin} and frequency of f_{sin} is fed to the CCOPA, the input of G_{m1} will only see a fraction of this sine wave A_{sin_Gm1} which can be calculated by the following:

$$A_{sin\_Gm1} = A_{sin}\frac{R_{b1,2}}{\left|j\omega C_{in1,2}\right| + R_{b1,2}} = A_{sin}\frac{R_{b1,2}}{\sqrt{\left(2\pi \times f_{sin} \times C_{in1,2}\right)^2 + R_{b1,2}^2}} \tag{3.6}$$

In order to keep the CCOPA working, A_{sin_Gm1} must be smaller than 1.4 V (p–p); otherwise, the protection diodes will turn on and clip the input of G_{m1}. As a result, the maximum amplitude and/or the frequency of the input CM signal are restricted by Eq. (3.6).

3.2 Capacitively Coupled Chopper IAs (CCIA)

The first CCIA was published by Denison in 2007 [6] for LV biomedical applications. However, this had a single-ended output. A simplified block diagram of a differential CCIA is shown in Fig. 3.2. It consists of a two-stage Miller-compensated opamp (G_{m1} and G_{m2}), an input chopper (CH_{in}), an output chopper (CH_{out}), a feedback chopper (CH_{fb}), and a capacitive network ($C_{in1,2}$ and $C_{fb1,2}$). An input DC signal is first up-modulated by CH_{in} and then converted into an AC current by $C_{in1,2}$. This AC current flows through $C_{fb1,2}$, creating an AC voltage, which is finally demodulated by CH_{fb}. As a result, a DC signal is obtained at the CCIA's output. And the gain of the CCIA is simply $C_{in1,2}/C_{fb1,2}$. To bias G_{m1} properly, two biasing resistors $R_{b1,2}$ are added at the input of G_{m1}. At steady state, the input CM voltage of G_{m1} thus equals to V_{ref} as shown in Fig. 3.2.

It is possible to make a single-ended CCIA, which is already introduced in Sect. 1.3. The drawback is reduced peak-to-peak output voltage swing, since a reference voltage (V_{ref} in Fig. 1.10) equal to about half the supply is usually employed. Moving CH_{out} to the output is also possible. In this case, CH_{fb} is no longer needed. However, the penalty is the reduced equivalent DC gain as explained in the case of a CCOPA.

3.2.1 Offset and 1/f Noise

Like the CCOPA, chopping up-modulates the offset and 1/*f* noise of G_{m1}, so that low offset and low 1/*f* noise are obtained.

3.2.2 Noise and Power Efficiency

To evaluate the power efficiency of the CCIA, the main noise sources must be analyzed first: the noise of G_{m1} and $R_{b1,2}$. For high power efficiency, G_{m1} should be

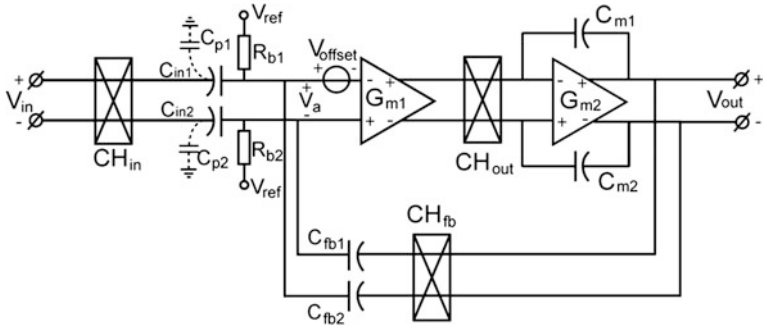

Fig. 3.2 A block diagram of a capacitively coupled chopper IA

biased in weak inversion. And its input-referred noise voltage V_{nGm1} can be calculated as follows [6]:

$$V_{nGm1} = \frac{C_{in1,2} + C_{fb1,2} + C_{p1,2}}{C_{in1,2}} \times V_{n1} \tag{3.7}$$

where $C_{p1,2}$ are the parasitic capacitors at the input of G_{m1}, which includes the gate capacitances of the input transistors, the parasitic capacitances associated with $C_{in1,2}$ between the virtual ground (V_a in Fig. 3.2) and ground, the layout parasitics. According to Eq. (3.7), the noise of the CCIA will be almost equal to the noise of G_{m1} when $C_{fb1,2}$ is much smaller than $C_{in1,2}$, provided $C_{p1,2}$ are also negligible compared to $C_{in1,2}$. Thus, the CCIA can be very power efficient with relatively high closed-loop gain ($C_{in1,2}/C_{fb1,2} > 5$). Like the CCOPA, the biasing resistors $R_{b1,2}$ also generate noise which can be calculated from Eq. (3.3). With a proper design of $R_{b1,2}$ and a relatively high closed-loop gain (>5), the CCIA's power efficiency can be optimal, i.e., close to that of a simple differential pair biased in weak inversion. This is a big advantage of the CCIA compared to the conventional topologies such as a three-opamp or current feedback topologies. In a classic three-opamp IA [7, 8], the noise is determined by at least two input buffers, while in a current feedback IA (Fig. 2.6 [9–11]), the noise is determined by an input and a feedback stage.

3.2.3 CMRR and CMVR

The CMRR of the CCIA is also quite high especially at DC as for a CCOPA.

Similarly, with a proper input chopper the CMVR of a CCIA can be potentially increased to the breakdown voltage of the input capacitors.

3.2.4 Gain Accuracy

A CCIA can achieve high gain accuracy since this depends on the mismatch between $C_{in1,2}$ and $C_{fb1,2}$. With careful layout and good lithography, a gain error close to 0.1 % can be achieved. When the voltage coefficient of the capacitors is low, this gain error becomes relatively independent of the input and output CM voltage difference of the IA. This is a big advantage of a CCIA compared to some other traditional IA topologies. For instance, the gain accuracy of a CFIA shown in Fig. 2.6 is dependent on its input and feedback transconductor mismatch and the accuracy of the resistor bridge. The transconductor mismatch usually has a strong dependence on the input and output CM voltage difference of the IA [9], which means that without special precautions, the gain accuracy will be limited to about 0.5 % in the presence of large input and output CM differences [10].

3.2.5 Input Impedance

The input chopper and input capacitors form an equivalent resistor, the DC resistance of which is calculated by the following:

$$Z_{\text{in\_DC}} = \frac{1}{2f_{\text{chop}} \times C_{\text{in1,2}}}. \tag{3.8}$$

Normally, $C_{\text{in1,2}}$ are in the order of a few Pico farad. And thus, the input impedance can be in the order of a few Mega Ohm to tens of Mega Ohm. Compared to a chopper CFIA with the same chopping frequency, the input impedance of a CCIA is thus $C_{\text{in1,2}}/C_{\text{p1,2}}$ times lower than that of the CFIA, where $C_{\text{p1,2}}$ is the input parasitic capacitance of the CFIA's input stage. This, however, is not a problem in applications where the source impedance is low. For instance, in the current-sensing applications which will be presented in Chap. 6, the source impedance will be no larger than a few hundreds of Ohm. Thus, the input impedance of a normal CCIA will be sufficient. However, in applications where the source impedance is much higher, the input impedance of the CCIA must be increased. A solution will be presented later in Chap. 7.

3.2.6 Output Spikes

When an output signal V_{out} is present, the feedback capacitors are sampling either $+V_{\text{out}}$ or $-V_{\text{out}}$ due to the feedback chopper. The charging and discharging currents required by this process thus introduce output spikes, since the output stage normally has a finite output impedance and current. The larger V_{out} is, the more charging and discharging currents are required, and thus, the bigger the output spikes are. These spikes are not desired in most applications and thus must be eliminated. Various solutions to this problem will be introduced in Chap. 6.

3.2.7 Settling and Transient Issues

Lastly, just like the CCOPA, the biasing resistors and the input capacitors limit the CM response at the virtual ground of the CCIA with a time constant calculated by Eq. (3.5).

3.3 Conclusions

From the above introductions, it is not difficult to conclude that both the CCOPA and CCIA can achieve microvolt offset and low $1/f$ noise. With proper design, low noise and low power consumption can be achieved simultaneously in the case of a

CCOPA. In the case of a CCIA, the same can be achieved with a closed-loop gain larger than about 5. Thanks to the input capacitor; high DC CMRR and CMVR can be expected. However, to withstand the high-input CM voltage, a special input chopper must be used. This will be discussed in details in Chap. 4. As mentioned earlier, the transient settling of both the CCOPA and CCIA is limited by the time constant determined by the biasing resistors $R_{b1,2}$ and input capacitors $C_{in1,2}$. Thus, care must be taken when fast signals (both differential and CM) are present. Finally, for a CCIA especially, high gain accuracy can be expected when capacitors with low voltage dependence are available. The output spikes, however, should be made negligible. A solution to this problem will be presented in Chap. 6.

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Chapter 4
Choppers for High Input Common-Mode Voltages

As described in Chaps. 1 and 3, capacitively coupled chopper amplifiers can potentially achieve an input CMVR equal to the breakdown voltage of their input capacitors. However, this cannot be realized without a high-voltage (HV) input chopper that is also able to handle such voltages. Although an isolation transformer can be used to drive the MOSFETs of a normal chopper (Sect. 1.2), this technique is not compatible with standard IC technology. Thus, other realizations must be found. One solution is to realize the chopper switches with HV transistors. However, the required gate control signals cannot be provided by standard low-voltage (LV) digital circuits, and so special level shifters are required. Another solution is to use a HV amplifier to "boost" the LV clock signal. This, however, consumes extra power. A better solution is to again employ capacitive coupling. A LV clock signal (swinging from 0 to 5 V) can then be superimposed on the input CM voltage and used to drive the gates of the HV switch transistors. In this chapter, the design of the chopper switches will be discussed. This is followed by a discussion of a number of HV chopper topologies, some of which are used in the amplifiers presented later in the thesis. Later, a discussion of circuits to protect the HV chopper from input transients will be given. The chapter ends in conclusions.

4.1 Choice of Transistors

In the 0.7-μm technology used for most of the amplifiers presented in this thesis, there are two types of HV transistors: DMOS transistors and floating HV NMOS transistors. In this section, the characteristics of these transistors and their suitability for use in a HV chopper will be discussed. Although 0.7-μm CMOS technology can be considered as rather old-fashioned, the similar types of transistors to be discussed in the following can be widely found in many more advanced technologies, making the discussion still relevant even if the reader is using a different technology.

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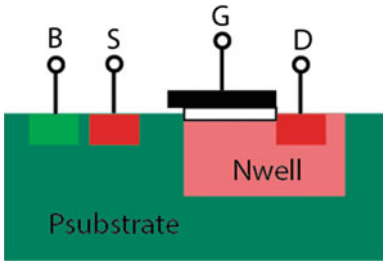

Fig. 4.1 Simplified cross section of a non-floating DMOS transistor

There are two types of DMOS transistors in 0.7-µm technology: the standard DMOS and the floating DMOS. In Fig. 4.1, a simplified cross section of a standard DMOS transistor is shown. Due to the extra N-well, a large drain–source breakdown voltage is obtained (up to 100 V). And thanks to a thick gate oxide, a large gate–source breakdown voltage (12 V) is also obtained. However, both source and drain terminals cannot be driven more than 0.7 V below the P-substrate. Thus, this type of transistors cannot be used when a large negative input CM voltage is present.

The cross section of a floating DMOS transistor is shown in Fig. 4.2. The major difference with the standard DMOS is that the source and bulk terminals are buried in an N-tub. In this way, they can be driven up to 100 V below the P-substrate. The isolation can be modeled by two junction diodes connected back-to-back, as shown in Fig. 4.2. D_{p1} represents the diode between the N-tub and the ground P-substrate, and D_{p2} represents the diode between the local P-well and the N-tub. However, the drain terminal is directly connected to the N-tub and cannot be driven more than 0.7 V below the P-substrate. Thus, this type of transistor also cannot be used in the presence of large negative CM voltages. When used in a chopper, the large drain–source breakdown voltage of a DMOS is not particularly advantageous since the drain–source voltage is defined by the amplitude of the differential input signal, which, in precision systems, is usually below 300 mV.

The floating HV NMOS transistor is a LV NMOS transistor that is situated in a HV N-tub. The cross section of a floating NMOS transistor is shown in Fig. 4.3. It consists of a LV NMOS transistor, a local P-substrate, and a HV N-tub which is surrounded by a common P-substrate connected to ground. The N-tub is capable of floating up to 100 V with regard to the P-substrate, and the local P-substrate is capable of floating down to at least −30 V with regard to the N-tub. Like the floating DMOS transistor,

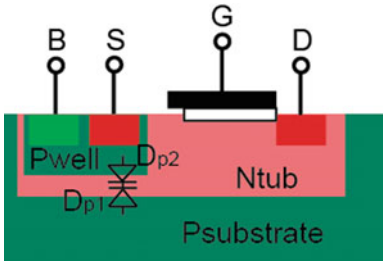

Fig. 4.2 Simplified cross section of a floating DMOS transistor

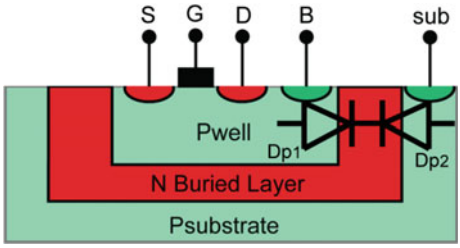

Fig. 4.3 Cross section of a HV floating NMOS transistor

this isolation can again be modeled by two junction diodes connected back-to-back, as shown in Fig. 4.3. When used in a chopper, the local P-substrate can be connected to the input of the chopper and the N-tub is left floating. When the potential of the local P-substrate rises with the CM input voltage, the potential of the N-tub will follow it; when the potential of the local P-substrate decreases with the CM input voltage, the potential of the N-tub will decrease but not further than 0.7 V below ground. In this way, the chopper switches can safely be operated at CM voltages ranging from −30 V to 100 V. The voltages between any two terminals (gate, drain, source, and bulk), however, must be restricted to less than 5 V.

To conclude, both DMOS and floating HV NMOS transistors can be used as HV chopper switches. However, when large negative CM voltages are expected, only floating HV NMOS transistors can be used. Another advantage of these transistors is their low resistance, around 4 kΩ/μm (@5 V V_{gs} and 0.2 V V_{ds}), which is much lower than the 40 kΩ/μm (@12 V V_{gs} and 0.2 V V_{ds}) of DMOS transistors. The threshold voltage of DMOS transistors is also higher than that of the floating HV NMOS transistors. As a result, the floating HV NMOS transistors are the preferred switches for a HV chopper. In next section, several HV chopper topologies will be introduced.

4.2 High-voltage (HV) Chopper Topologies

4.2.1 HV Chopper with HV Amplifier Level-Shifter

A HV chopper using a HV amplifier level-shifter has been described by C. Birk in [1]. A simplified schematic of the chopper is shown in Fig. 4.4. Although the chopper switches in [1] were realized by DMOS transistors, the concept of this topology can be applied to other types of transistors. With the complementary clock signal applied to MN_1 and MN_2, an amplified clock signal is obtained at node A. However, the maximum gate–source voltage of the DMOS transistors used in [1] is only 5 V. Thus, the clock swing at node A must be limited. By using MN_3, the lowest gate–source voltage of $MNs_{1,2}$ is limited to $-V_{thn3}$ (threshold voltage of MN_3); and by employing D_{1-3} and MP_1, the maximum gate–source voltage of $MNs_{1,2}$ is limited to $3V_{thd} + V_{thp}$ (where V_{thd} is the threshold voltage of D_{1-3}, and V_{thp} is the threshold voltage of MP_1).

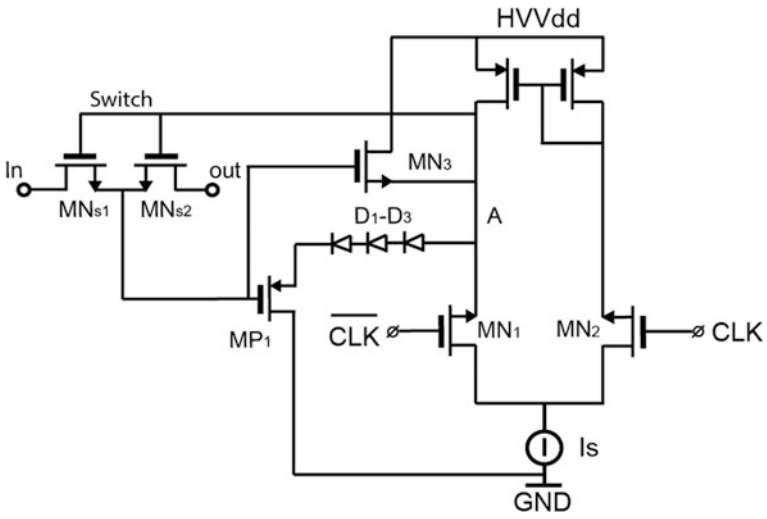

Fig. 4.4 Schematic of a HV chopper switch driven by HV amplifier level-shifter by Birk [1]

The main drawback of this approach is that a certain amount of bias current I_s must be drawn from a high supply voltage. Thus, more power consumption and an extra pin for the high supply voltage are required. To overcome these drawbacks, the HV amplifier level-shifter should be eliminated, e.g., by using capacitive coupling. In the following section, a number of capacitively coupled HV choppers will be introduced.

4.2.2 Capacitively Coupled HV Choppers

The basic capacitively coupled chopper is shown in Fig. 4.5. The clock signal is AC-coupled to the gates of the four chopper switches via four capacitors, C_{11-14}. The DC level of the gates, however, is undefined and so must be fixed properly. This can be done by adding diodes around the chopper switches as shown in Fig. 4.6. Two sets of diodes (forward and reverse) are connected to the gates of every switch. The "reverse" diodes connected from the source to the gate ensure that the gate voltage is always less than about 0.7 V below the source voltage. And the "forward" diodes connected from the gate to the drain ensure that the gate voltage never rises more than 2.1 V above the drain. Different numbers of forward and reverse diodes can be used. However, it is best to use just one reverse diode, since more diodes will result in an unnecessary loss of overdrive voltage. The number of forward diodes depends on the supply voltage and the desired overdrive voltage.

In the particular case shown in Fig. 4.6, the gate source/drain voltages of the chopper switches switch between −0.7 V and 2.1 V when the clock signal

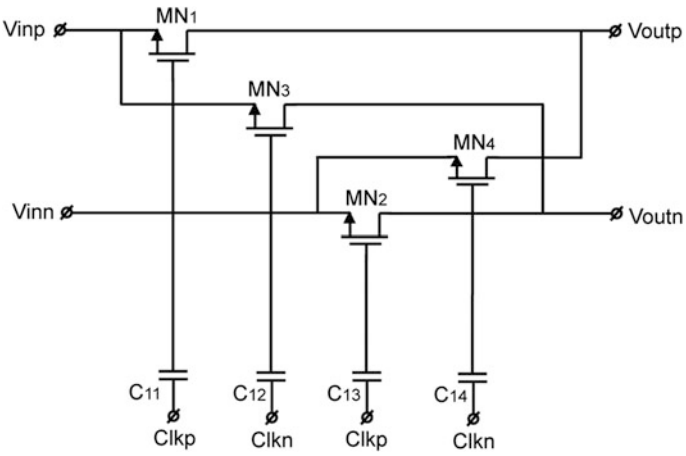

Fig. 4.5 Schematic of a capacitively coupled chopper

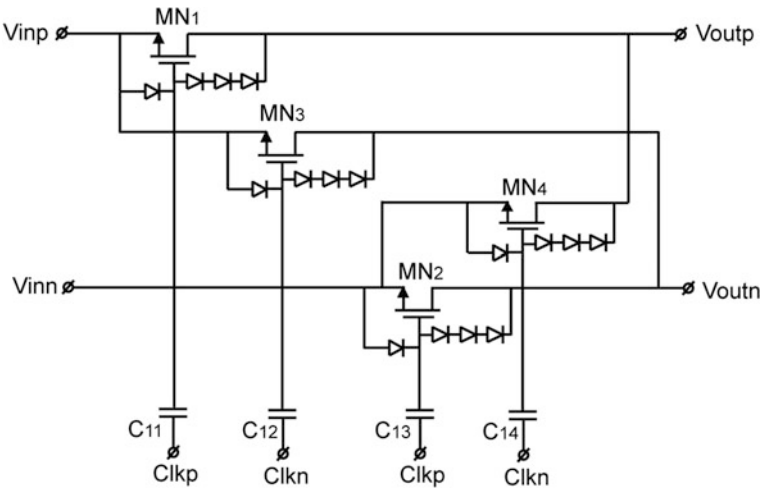

Fig. 4.6 Schematic of a capacitively coupled chopper with diodes

amplitude is greater than 2.8 V. As a result, the overdrive voltage of the chopper switches is fixed and independent of the input CM voltage. Thus, unlike a standard chopper (Fig. 2.1), the overdrive voltage of a capacitively coupled chopper is independent of the input CM voltage, and thus, the chopper is essentially free of CM-voltage-dependent charge injection and clock feed-through.

However, this circuit still has a problem. When the clock signal amplitude is lower than 2.8 V, the gate voltages will float somewhere between −0.7 V and 2.1 V with an amplitude almost equal to the clock signal. In this case, the overdrive voltage of the chopper switches will not be well defined.

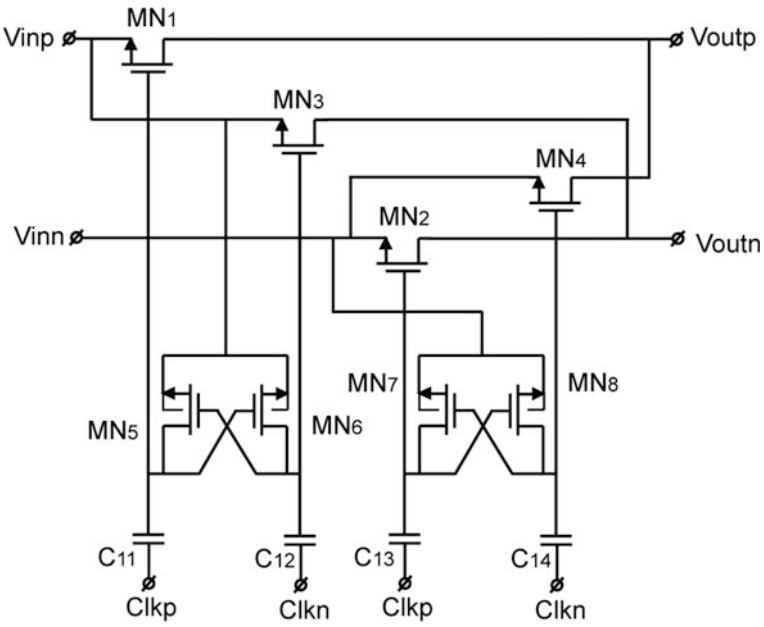

Fig. 4.7 Schematic of a capacitively coupled chopper with latches

To avoid this situation, the diodes can be replaced by latches, which then fix the DC level of the switches' gate voltages. This solution is shown in Fig. 4.7 [2]. During one clock transient, MN_5 and MN_7 are turned on, and the gate voltages of MN_1 and MN_2 become equal to the CM input voltage (V_{inp} and V_{inn}, respectively). During the next clock transient, MN_6 and MN_8 are turned on, and the gate voltages of MN_3 and MN_4 become equal to V_{inp} and V_{inn}, respectively. Meanwhile, the clock signal is coupled to the gates of MN_1 and MN_2 via coupling capacitors C_{11} and C_{13}. After a few cycles, the clock signals at the gates of MN_1–MN_4 will switch between V_{inp} and V_{inn} with a certain amplitude V_{cclk}. This amplitude V_{cclk} is determined by the ratio between the coupling capacitors C_{11-14} and the gate parasitic capacitances C_p of each chopper switch and can be written as:

$$V_{cclk} = V_{clk} \frac{C_{11}}{C_{11} + C_p}, \tag{4.1}$$

where V_{clk} is the amplitude of the coupled clock signal, which is generally equal to the supply. It is worth pointing out that this equation is also applicable to other capacitively coupled choppers, such as the one shown in Fig. 4.6.

With the diodes replaced by the latches, the gate voltage of the chopper switches is always higher than V_{inp}/V_{inn} and so is not floating. The design can be simplified by tying the gates of MN_1 (MN_3) to that of MN_2 (MN_4) as shown in Fig. 4.8 [3]. This, however, introduces asymmetry in the chopper, since the charge injection and

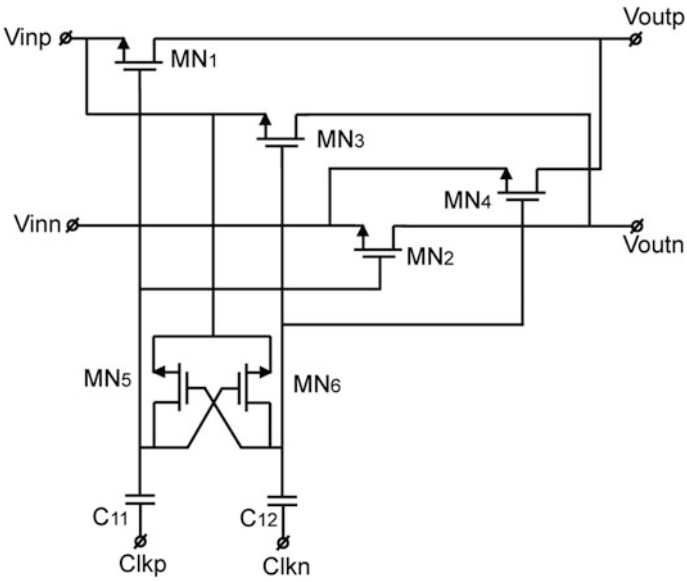

Fig. 4.8 Schematic of the capacitively coupled chopper with all NMOS transistors

clock feed-through errors of the latch ($MN_{5–6}$) will be injected only into terminal V_{inp}.

One drawback of capacitively coupled choppers with latches, however, is that the input signal must be smaller than roughly 0.3 V. This is because the reference of the latch is tied to one of the inputs. Thus in Fig. 4.8, for instance, when V_{inp} = 1 V and V_{inn} = 0 V, the gate voltages of all the switches will exceed 1 V. As a result, MN_2 and MN_4 will never turn off.

For large signals, the chopper of Fig. 4.8 can be modified as shown in Fig. 4.9 [4]. The added structure is called a minimum selector, as it selects the lowest input voltage. The reference of the latch is connected to the output of the minimum selector (point A). Now when V_{inp} = 1 V and V_{inn} = 0 V, MN_8 will be turned on, and the voltage at point A will be 0 V, thus setting the reference of the latch to 0 V. As a result, all the transistor switches can now be turned off.

4.3 Transient Protection

In the presence of large transient signals, the chopper's NMOS transistors must be protected, since they are actually LV transistors and so the voltage between any two of their terminals must be restricted to less than 5 V.

Taking the chopper of Fig. 4.8 as an example, two protection diodes $D_{1,2}$ are added as shown in Fig. 4.10 [3]. In the absence of clock signals, the diodes D_1 and

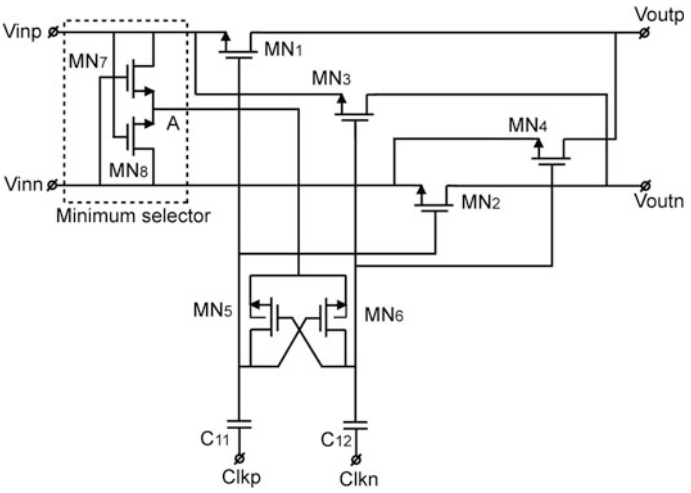

Fig. 4.9 Schematic of the capacitively coupled chopper with minimum selector

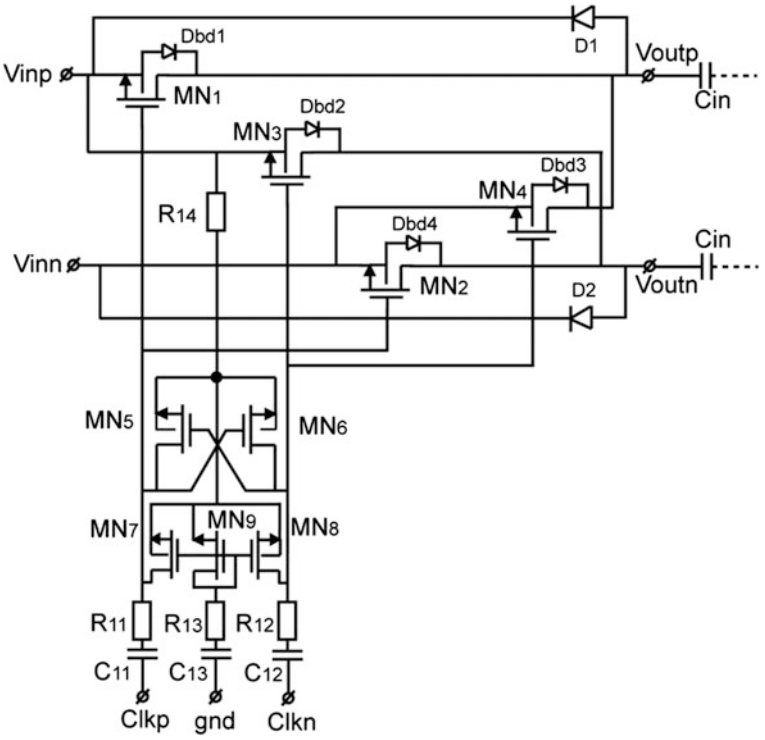

Fig. 4.10 Schematic of the capacitively coupled chopper with protection circuits

D_2 ensure that the output of the chopper follows the input when the CM input voltage decreases rapidly. Furthermore, the bulk–drain diodes of $MN_{1–4}$ limit the drain–source voltages of the corresponding transistors to 0.7 V when the CM input voltage increases rapidly.

To protect the gates of the chopper switch transistors, a model circuit consisting of $MN_{7–9}$ is added, as shown in Fig. 4.10. As the CM input voltage increases, the bulk–drain diodes of $MN_{7,8}$ ensure that the gates of $MN_{1–4}$ are not more than 0.7 V lower than V_{inp}. If the input CM decreases, MN_9 is turned on which increases the voltage drop across C_{13}. This action is then mirrored by $MN_{7,8}$, which force the gates of $MN_{1–4}$ to follow V_{inp}. Moreover, if the clock signals overlap briefly, both MN_5 and MN_6 will be on for a short moment. During this moment, a relatively large transient current will occur, which will be injected into the V_{inp} terminal (Fig. 4.10). To limit this current spike, resistors R_{11}–R_{14} can be added.

Similar protection schemes can be applied to all the other choppers introduced above.

4.4 Conclusions

The capacitively coupled choppers presented in this chapter can be used in a variety of applications in which the CM input voltage does not exceed the breakdown voltage of the floating N-tub. If the input signals are small (<300 mV), then the choppers of Figs. 4.7 and 4.8 can be used, while for larger signals the chopper in Fig. 4.9 can be used. In both cases, the protection diodes and current limiting resistors introduced in Sect. 4.3 (Fig. 4.10) can be used to protect the choppers during large input voltage transients.

Having presented the design of suitable HV choppers, we are now ready to discuss their application in capacitively coupled chopper amplifiers that are capable of handling large (beyond-the-rail) CM voltages. This will be the topic of Chaps. 5 and 6.

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2. Q. Fan, J. H. Huijsing, K.A.A. Makinwa, “A Capacitively-Coupled Chopper Operational Amplifier with 3μV Offset and Outside-the-Rail Capability,” *Proc. ESSCIRC,* pp.73-76, Sept. 2012.
3. Q. Fan, J. H. Huijsing, K. A. A. Makinwa, “A capacitively-coupled chopper instrumentation amplifier with a ±30V common-mode range, 160dB CMRR and 5μV Offset,” *IEEE ISSCC Dig. Tech. Papers*, pp. 374-376, Feb. 2012.
4. J. H. Huijsing, Q. Fan, K. A. A. Makinwa, D. Fu, S. Wu, J. Wu, Y. Chen, “Fully capacitive coupled input choppers”, US patent in process.

Chapter 5
Capacitively-Coupled Chopper Operational Amplifiers

In Chap. 3, the basic capacitively-coupled chopper topology for operational amplifiers (opamp) has been described. In this chapter, two capacitively-coupled chopper opamps (CCOPA) will be presented. They both achieve wide input common-mode voltage range (CMVR) and high precision. The first opamp employs a single-path architecture and features high power efficiency and simplicity. The second opamp is more complex and employs a multipath architecture. Thus, it is less power efficient, but has a wider bandwidth and a smoother transfer function.

5.1 Introduction

An opamp is a basic building block of analog circuit design and is often used to implement instrumentation amplifiers (IAs), integrators, filters, comparators, and so on. To satisfy the needs of such diverse applications, a wide input CMVR is preferred. Conventional techniques for extending the CMVR of an opamp include the use of a complementary input stage or the use of a charge pump (or a HV supply) to power a simple differential pair. These approaches, however, all significantly increase the opamp's power consumption. Thus, a more power efficient way of achieving wide CMVR is required. Moreover, when used in precision measurement systems, microvolt offset and high common-mode rejection ratio (CMRR) are required. To simultaneously obtain wide input CMVR, high power efficiency, and precision, a CCOPA is proposed, whose basic working principle has been introduced in Chap. 3. This allows the opamp's CMVR to be extended maximally to the breakdown voltage of the input capacitors without any extra power dissipation. When combined with chopping, microvolt offset and high CMRR can be expected as explained in Chaps. 2 and 3. Chopping introduces ripple which must be suppressed, and this is done by employing a ripple-reduction loop (RRL). The RRL, however, creates a notch in the opamp's transfer function as explained in Chap. 2. Moreover, an input signal at f_{chop} can be demodulated by the input chopper and then blocked by

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the input capacitors (Fig. 3.1). To overcome these problems, a multipath CCOPA is proposed, which achieves a smooth transfer function, an output step response without significant chopper ripple, and wider bandwidth.

In Sect. 5.2, the traditional techniques to boost the input CMVR are first introduced. Then, the design of a single-path CCOPA will be described from system level to transistor level in Sect. 5.3, followed by the measurement results. Later, a multipath CCOPA will be described in Sect. 5.4, with system-level, transistor-level design considerations and experimental results. This chapter ends in conclusions.

5.2 Conventional Techniques to Expand the CMVR

Two techniques that are often used to extend CMVR are as follows: the use of a complementary input stage [1–4] and the use of a charge pump [5–7] or an extra HV supply. A complementary input stage is shown in Fig. 5.1. It consists of an NMOS and a PMOS differential pair in parallel. A folded-cascode stage then sums up the signal currents of the NMOS and PMOS input pairs. The NMOS pair has an input CMVR from V_N to *Vdd*; where V_N is the voltage at which the NMOS pair is turned on. While the CMVR of the PMOS pair is from GND to V_P; where V_P is the voltage at which the PMOS pair is active. When $V_N \leq V_P$, the input CMVR of the amplifier will be rail-to-rail. However, when $V_N > V_P$, a deadband will be formed, during which neither the NMOS or the PMOS pairs will be turned on.

A charge pump is shown in Fig. 5.2. In Φ_1, *Vdd* is converted into a charge and stored on capacitor C; and in Φ_2, this charge is redistributed between C and C_L;

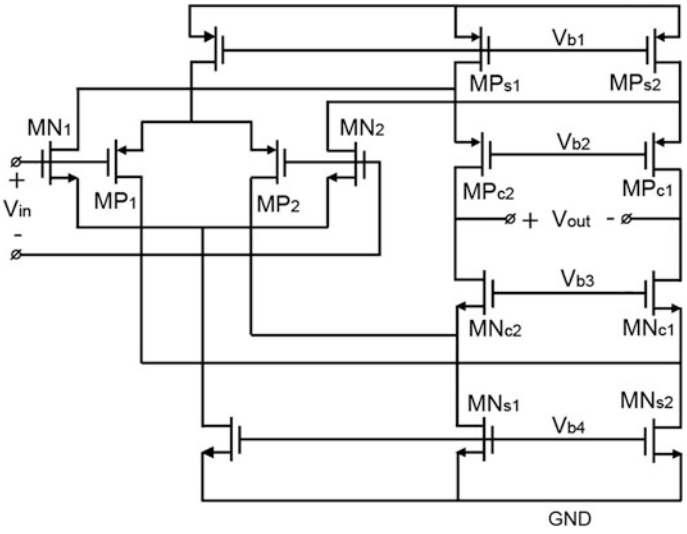

Fig. 5.1 A complementary input stage with a folded-cascode stage

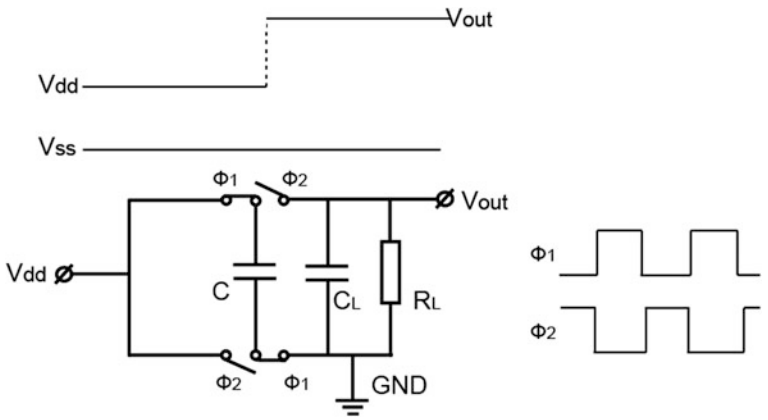

Fig. 5.2 A basic charge pump with load resistor and a load capacitor

thus, the voltage stored on C_L (V_{out}) is increased. After several clock cycles, V_{out} will be gradually equal to $2Vdd$. Thus, when a PMOS differential pair is powered by V_{out}, its CMVR can extend from GND to a voltage somewhat higher than Vdd. Rather than implementing a charge pump, whose clock frequency may then leak into the input signal, an extra HV supply can also be used.

Nowadays, power efficiency is required in most applications, and so the input stage usually consumes most of the supply current. Both of the techniques described are rather power inefficient: The use of a complementary input stage doubles the supply current, while the use of a charge pump or an external HV supply raises the voltage applied to the input stage and thus its power consumption.

5.3 The Single-Path Capacitively-coupled Operational Amplifier (CCOPA)

In this section, the design and implementation of the single-path CCOPA will be given. Later, the experimental results will also be shown.

5.3.1 Design of the Single-Path CCOPA

A simplified schematic of the CCOPA (for the basic operation see Chap. 3) is shown in Fig. 5.3. It consists of an input chopper CH_{in}, an output chopper CH_{out}, two HV input capacitors C_{in11} and C_{in12}, an input transconductor $G_{m1,}$ and a nested-Miller integrator built around G_{m2} and G_{m3}. The input differential signal is first up-modulated by CH_{in}, converted into a current by the input transconductor G_{m1}, then demodulated back to baseband by CH_{out}, and finally integrated by the

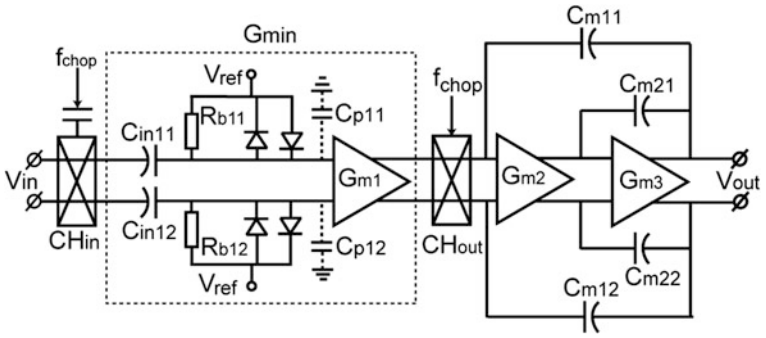

Fig. 5.3 Schematic of the basic CCOPA

integrator built around G_{m2} and G_{m3}. With the HV input capacitors and the floating input chopper, the CMVR of the CCOPA is greatly extended. The input CM DC level of G_{m1}, however, is fixed by the biasing resistors $R_{b11,2}$ to V_{ref}. Thus, G_{m1} is powered by low supply voltage, and no HV transistors are required. To protect G_{m1} in the presence of a large CM transient voltage step, four protection diodes are added in parallel with $R_{b11,2}$. In this way, the CM input voltage of G_{m1} can never exceed $V_{ref} \pm 0.7$ V.

5.3.1.1 Frequency Compensation of the CCOPA

As shown in Fig. 5.3, the CCOPA employs three gain stages to ensure high DC gain. Thus, nested-Miller compensation is employed to ensure its stability, which normally requires the following equation to be fulfilled [1]:

$$\frac{G_{m1}}{C_{m1}} \leq \frac{1}{2}\frac{G_{m2}}{C_{m2}} \leq \frac{1}{4}\frac{G_{m3}}{C_l} \tag{5.1}$$

In this work, the CCOPA is designed to be conditionally stable for a closed-loop gain higher than 20, since it's main application is precision amplification. As a result, Eq. (5.1) can be relaxed and the following equation should be satisfied:

$$\frac{G_{m1}}{C_{m1}} \leq \frac{1}{2}\frac{G_{m2}}{C_{m2}} \leq \frac{1}{4}\frac{G_{m3}}{C_l} \times 20 \tag{5.2}$$

One consideration, however, is focused on the position of the dominant pole. Since the CCOPA is designed for precision applications, its input-referred noise should be minimized. Thus, the input transconductance G_{m1} should be maximized. Meanwhile, a relatively small G_{m2} is preferred to save power consumption. As a result, according to Eq. (5.2), C_{m1} has to be much larger than C_{m2}, which leads to extra chip area. The solution to this problem is to swap the positions of the poles associated with G_{m1} and G_{m2}, which means that Eq. (5.2) can be modified as follows:

$$\frac{G_{m2}}{C_{m2}} \leq \frac{1}{2}\frac{G_{m1}}{C_{m1}} \leq \frac{1}{4}\frac{G_{m3}}{C_l} \times 20 \tag{5.3}$$

In this way, the dominant pole is no longer defined by G_{m1} and C_{m1}, but rather by G_{m2} and C_{m2}. Thus, a relatively small G_{m2} can be employed to save power consumption, and a relatively small C_{m1} can be used to save chip area. The slew rate of the circuit, however, may be limited by G_{m2} and $C_{m21,2}$. Thus, to enhance the slew rate, the output current that G_{m2} is able to deliver must be optimized. However, the same story also applies to G_{m1}, since a signal current is required to charge $C_{m1,2}$ as well.

5.3.1.2 Input Chopper

Several floating choppers with beyond-the-rail CMVR have been introduced in Chap. 4: two small-signal topologies (Figs. 4.7 and 4.8) and a large signal topology (Fig. 4.9). For a CCOPA, the input differential signal is always small since its input will serve as a virtual ground. Thus, one of the small-signal topologies can be used. The symmetry of the chopper, however, is important. When the CCOPA is used with a resistive feedback network as shown in Fig. 5.4, any asymmetrical charge injection and clock feed-through spikes will be transferred to the input of the amplifier via the input resistors $R_{in11,2}$. As the resistance increases, the input-referred errors increase. To minimize this error, the input chopper should be as symmetrical as possible. And thus, the fully symmetrical chopper for small signals shown in Fig. 4.8 is most suitable for a CCOPA.

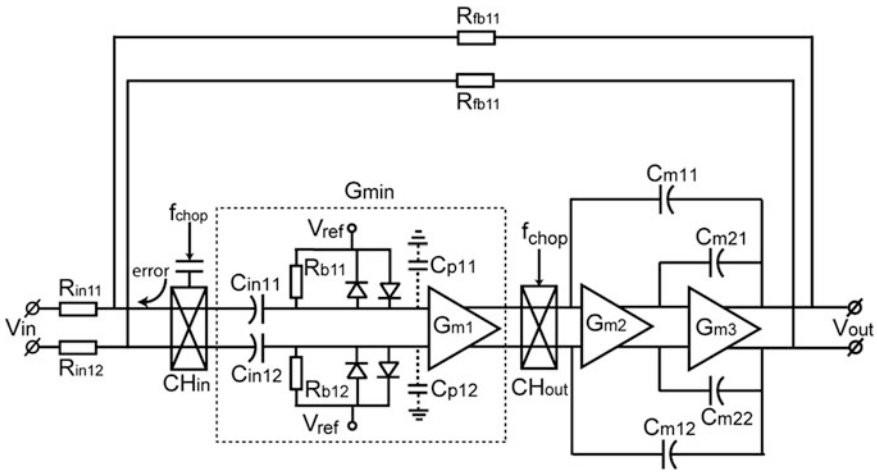

Fig. 5.4 Schematic of the basic CCOPA with resistive feedback network

5.3.1.3 Switched-Capacitor Ripple-Reduction Loop (SC RRL)

In a chopper amplifier, the up-modulated offset and 1/*f* noise cause ripple. To suppress this, a ripple-reduction loop (RRL) can be employed. The working principle of a RRL has already been introduced in Chap. 2 (Fig. 2.9). However, the RRL presented in Chap. 2 is not very practical because the offset of the RRL integrator G_{m3} will, via $C_{s1,2}$, give rise to large residual ripple. To eliminate this offset, the integrator can be auto-zeroed. However, a standard auto-zeroed integrator must be reset within one clock phase so that its offset can be stored on an auto-zero capacitor. During that phase, the output of the integrator is equal to its offset voltage and cannot be used to compensate for the offset of the CCOPA's input stage. To solve this problem, a modified auto-zeroed integrator is proposed. A block diagram of the RRL with this integrator is shown in Fig. 5.5. The SC integrator comprises of sensing capacitors $C_{s1,2}$; a demodulation chopper CH_{RRL}; integration capacitors $C_{int1,2}$; auto-zero capacitors $C_{az1,2}$; and a single stage opamp G_{m5}. CH_{RRL} is synchronized to f_{chop}. The rest of the switches (S_1–S_6) are driven at a switching frequency f_s, which is chosen to be half of f_{chop}. The two half cycles of f_s serve as an integration phase Φ_1 and an auto-zero phase Φ_2, respectively, with each phase incorporating a complete cycle of f_{chop}. Thus, during Φ_1, a full cycle ripple can be detected by the RRL. A timing diagram is shown in Fig. 5.5. During Φ_1, $C_{s1,2}$ converts the ripple voltage into an AC current, which is then demodulated by

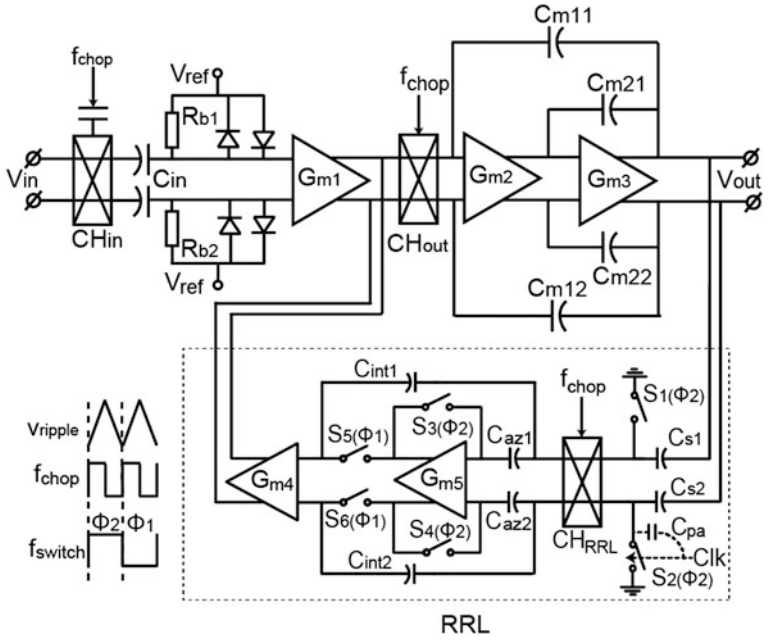

Fig. 5.5 CCOPA with a new switched-capacitor ripple-reduction loop

CH_{RRL} and integrated on $C_{int1,2}$. The voltage on $C_{int1,2}$ is then converted into a current by G_{m4} to compensate for the offset current of G_{m1}. During Φ_2, $C_{s1,2}$ is shorted to ground so that no ripple current is integrated. G_{m5} is configured in a unity-gain configuration so that its offset is sampled and stored on $C_{az1,2}$. During this time, $C_{int1,2}$ is disconnected from the output of G_{m5}, holding the voltage set at the end of the final Φ_1, and then connected to the input of G_{m4}. In this way, the correct compensating current is steadily injected into G_{m1} during both phases. In the ideal case, the compensating current fully compensates for the offset current of G_{m1}, leaving no output ripple at steady state.

It would also be possible to choose f_S equal to $2f_{chop}$. The difference is then that instead of a full cycle of ripple, only a quarter cycle of the ripple is detected during one switching cycle. However, this choice will increase the power consumption of the integrator opamp, since its bandwidth must be at least 5 × higher than f_S. An even lower f_S is also possible, but any switching non-idealities such as charge injection and clock feed-through associated with S_1–S_6 could result in residual ripple at f_S. This residual ripple can only be filtered by the CCOPA itself. Thus, decreasing f_S too much is undesirable.

The noise of the RRL can be designed to be negligible. This can be done by choosing a much smaller G_{m4} than G_{m1} as explained in Sect. 2.3. The SC integrator built around G_{m5} contributes noise, which includes both the noise of G_{m5} and the KT/C noise of the switches. However, this noise can often be neglected. This is because when referred to the output of the integrator, this noise will be shaped by a sinc function [8] and thus exhibit much more noise in low frequencies and much less noise in high frequencies. The noise at low frequencies is then suppressed by a rather small G_{m4}, up-modulated by CH_{out}, and then filtered by the integrator built around G_{m2} and G_{m3}. As a result, the noise of this SC integrator can often be made quite negligible.

5.3.2 *Implementation of the Basic CCOPA*

In this session, important implementation details with regard to the input CM biasing of G_{m1}, the transistor-level design of G_{m1}, G_{m2}, G_{m3}, input floating chopper, and the SC RRL will be given.

5.3.2.1 Global Parameters (f_{chop} and $C_{in1,2}$)

f_{chop} is an important design parameter, which, however, is not always easy to choose. Several factors should be taken into account. First, f_{chop} should be far away from the signal bandwidth, since the RRL will introduce a notch at f_{chop} in the CCOPA's transfer function (Sect. 2.3). Second, f_{chop} should be higher than the $1/f$ noise corner of G_{m1}, which is in this case $\sim$5 kHz, so as to fully remove the $1/f$ noise from the signal band. Third, as explained in Chap. 2, the residual offset depends on the charge

injection and clock feed-through errors of the chopper switches. Thus, a relatively low f_{chop} is preferred to achieve a low residual offset. A fourth consideration is the residual chopper ripple, which is due to the non-idealities of the RRL. With low f_{chop}, these errors become larger and more difficult to filter. Based on these considerations, f_{chop} is chosen to be 25 kHz in this work. Later, measurement results will prove that this choice results in sufficient $1/f$ noise suppression, and a good combination of both low residual offset and low residual ripple.

The choice of the value of the input capacitors $C_{in1,2}$ is also not straightforward. The main function of $C_{in1,2}$ is to isolate the input CM voltage; thus, theoretically, any value will do. However, in practice, there are several considerations. First, to save chip area, $C_{in1,2}$ should be minimized. Second, a compromise must be made between the input-referred noise of the biasing resistors $R_{b1,2}$ and the time constant determined by $R_{b1,2}$ and $C_{in1,2}$. This has been explained in detail in Chap. 3. To reduce the input-referred noise of $R_{b1,2}$, $C_{in1,2}$ should be large. However, for a fast CM settling at the input of G_{m1}, $C_{in1,2}$ should be small. Last but not least, the input impedance of the CCOPA is determined by f_{chop} and $C_{in1,2}$. And thus, $C_{in1,2}$ should be relatively small to obtain a high input impedance. In this work, low noise is very important since the CCOPA is intended for precision measurements. The input impedance, however, is not so critical since the input of the CCOPA will serve as a low-impedance virtual ground, which is guaranteed by its high open-loop gain. As a result, $C_{in1,2}$ are chosen to be relatively large: 8 pF. The chip area consumed by $C_{in1,2}$, however, is still acceptable. The CM settling time at the input of G_{m1} is also determined by $R_{b1,2}$, which will be discussed later.

5.3.2.2 Implementation of the Input Chopper

A schematic of the input chopper is shown in Fig. 5.6. For its implementation, the following three points were considered: charge injection and clock feed-through errors, noise contribution, and transient protection during large CM input. Charge injection and clock feed-through errors are already suppressed by the symmetrical design of the chopper. This, however, is only guaranteed by careful layout. Furthermore, the size of the NMOS transistors $MN_{5–14}$ should be minimized. To ensure that the input chopper does not contribute significant voltage noise, $MN_{1–4}$ are chosen to be relatively large (W/L = 6/0.7) to achieve a low on-resistance. The overdrive clock signal is determined by Eq. (4.1) and is roughly 2.5 V according to post-simulation. The resulting on-resistance of $MN_{1–4}$ is thus $\sim$1 kΩ, whose noise contribution is then negligible. Finally, the value of the protection resistors R_{11}–R_{14} is chosen to be 50 kΩ.

5.3.2.3 Implementation of the Gain Stages (G_{m1}, G_{m2}, and G_{m3})

The CCOPA is intended for precision measurements and thus its input-referred noise should be minimized for a given power consumption. As a result, the input

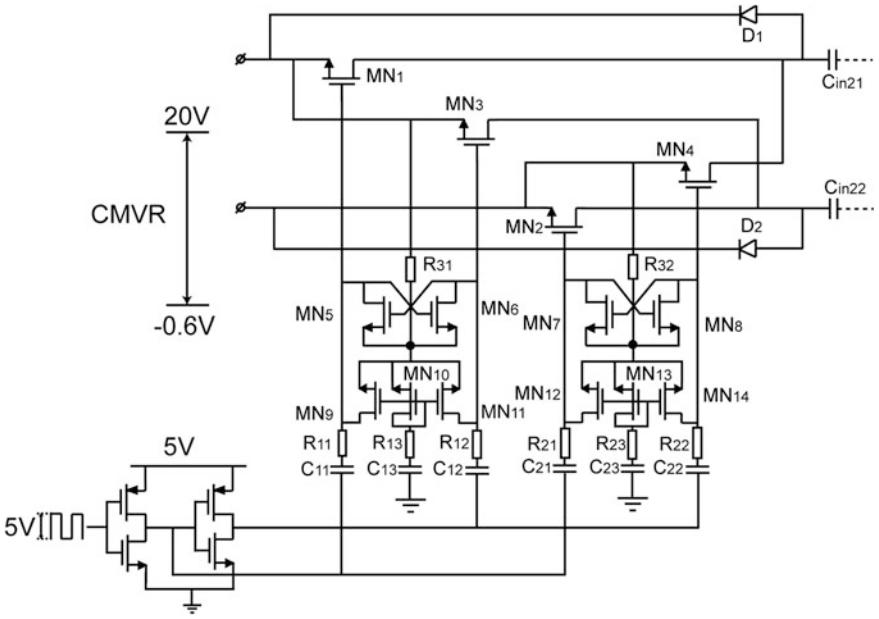

Fig. 5.6 Schematic of the input floating chopper

stage G_{m1} employs a simple PMOS differential pair, which is biased in weak inversion. G_{m2} employs a folded-cascode topology. The schematic of G_{m1} and G_{m2} are shown in Fig. 5.7. It can be seen that the input stage of the common-mode feedback (CMFB) circuit of G_{m1} is taken from the input stage of G_{m2} rather than directly from the output of G_{m1}. This is because the offset of G_{m2} (V_{os2}) will be chopped by CH_{out} and will appear as a square wave over the parasitic capacitor C_{p21-3}. The currents required to charge and discharge C_{p21-3} require an AC voltage at the input of G_{m1}. This AC voltage is demodulated to DC by CH_{in} and appears as a residual offset V_{os1}, which can be estimated by [9]

$$V_{os1} = \frac{4V_{os2}f_{chop}C_{p2}}{G_{m1}} \tag{5.4}$$

where $C_{p2} = C_{p22}+(C_{p21} + C_{p23})/2$. For V_{o2} = 10 mV, f_{chop} = 25 kHz, C_{p2} = 1 pF, and G_{m1} = 23 μS, V_{os1} is around 43 μV. To reduce this effect, C_{p2} must be minimized. As a result, the input of the CMFB circuit of G_{m1} has been shifted from the output of G_{m1} to the input of G_{m2}. Also, the size of cascoding transistors $MN_{c1,\ c2}$ and $MP_{c1,\ c2}$ has been minimized to reduce C_{p2}. For improved common-mode stability, the NMOS current sources have been split into $MN_{cm1,\ cm2}$ and $MN_{b1,\ b2}$ with a ratio of 1:2. Finally, the floor plan was optimized to minimize parasitic routing capacitances.

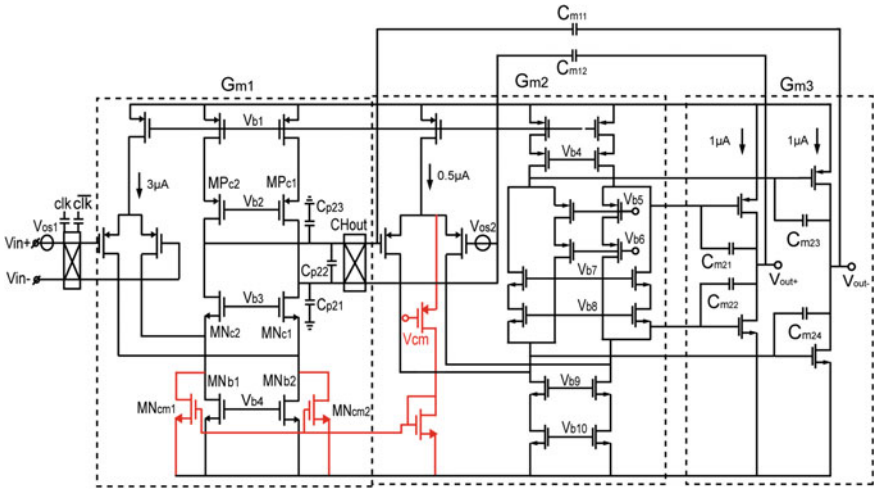

Fig. 5.7 Schematic of G_{m1}, G_{m2}, and G_{m3}

As mentioned before, the CCOPA is designed to be stable for a closed-loop gain higher than 20, and Eq. (5.3) should be satisfied. With G_{m1} = 28 μV, G_{m2} = 3.2 μV, G_{m3} = 23 μV, C_{m1} = C_{m2} = 13.5 pF, and an expected load capacitance C_l around 70 pF, Eq. (5.3) can be fulfilled. It is not difficult to find that the above parameters are not only designed to satisfy Eq. (5.3). With G_{m1} = 28 μV, the simulated input-referred noise is around 40 nV/$\sqrt{\text{Hz}}$. With C_{m1} = 13.5 pF, the bandwidth of the CCOPA is roughly 16.5 kHz (with a closed-loop gain of 20), which is smaller than f_{chop}. As a result, the notch introduced by the RRL at f_{chop} can be outside the signal band of the CCOPA. Moreover, the total in-band noise voltage of the CCOPA is ~5 μV, which is comparable to the targeted input-referred residual offset (<10 μV). G_{m2} is made relatively small to save power consumption. And, G_{m3} employs a class-AB output stage to ensure a good driving compatibility. A schematic of G_{m3} is shown in Fig. 5.7.

5.3.2.4 Implementation of the Input CM Biasing Resistors

The biasing resistors $R_{b1,2}$ shown in Fig. 5.3 define the input CM voltage of G_{m1}. As explained in Chap. 3, they also contribute input-referred voltage noise and influence the CM settling time at the input of G_{m1}. With f_{chop} = 25 kHz and $C_{in1,2}$ = 8 pF, $R_{b1,2}$ are chosen to be 50 MΩ, whose input-referred noise voltage can then be calculated by Eq. (3.3) and is 14.4 nV/$\sqrt{\text{Hz}}$. This is negligible compared to the input-referred noise of G_{m1} (40 nV/$\sqrt{\text{Hz}}$). The CM settling time can then be calculated from Eq. (3.8) and is ~400 μs. The large resistors are implemented by two NMOS transistors biased in subthreshold region [10] and are shown in Fig. 5.8.

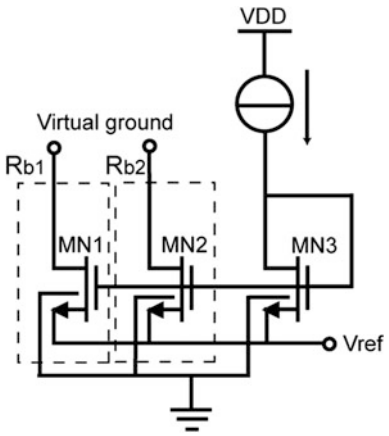

Fig. 5.8 Schematic of the implementation of the biasing resistors $R_{b1,2}$

5.3.2.5 Implementation of the SC RRL

The block diagram of the RRL is shown in Fig. 5.5. The RRL creates a notch whose bandwidth is given by [11]:

$$f_{0\mathrm{RRL}} = \frac{G_{\mathrm{m4}} C_{\mathrm{s}}}{2\pi C_{\mathrm{m1}} C_{\mathrm{int}}}, \tag{5.5}$$

where $f_{0\mathrm{RRL}}$ is half of the notch width. With $G_{\mathrm{m4}} = 1.26\ \mu\mathrm{S}$, $C_{\mathrm{s}} = 2$ pF, $C_{\mathrm{int}} = 4$ pF, and $C_{\mathrm{m1}} = 13.5$ pF, $f_{0\mathrm{RRL}}$ is calculated to be around 7.4 kHz. With a minimum closed-loop gain of 20, the bandwidth of the CCOPA is $\sim$16.5 kHz. Thus, the notch generated by the RRL is outside the bandwidth of the CCOPA, which is at $f_{\mathrm{chop}} = 25$ kHz. To make the noise of the RRL negligible compared to that of G_{m1}, G_{m4} is designed to be 22 × smaller than G_{m1}. C_{az} is chosen to be 1.4 pF, which is a compromise between the voltage error generated by charge injection and clock feed-through and chip area.

G_{m5} employs a telescopic topology, which is shown in Fig. 5.9. The ripple suppression factor F of the RRL is as follows:

$$F = \frac{A_{G\mathrm{m5}} G_{\mathrm{m4}}}{2 C_{\mathrm{m1}} f_{\mathrm{chop}}}, \tag{5.6}$$

where $A_{G\mathrm{m5}}$ is the open-loop gain of G_{m5}. The open-loop gain of the G_{m5} is simulated to be around 80 dB. To determine whether this suppression factor is enough, the unsuppressed ripple should be calculated assuming the offset of G_{m1} is 5 mV:

$$V_{\mathrm{ripple}} = \frac{V_{\mathrm{offset}} \cdot G_{\mathrm{m1}}}{2 f_{\mathrm{chop}} \cdot C_{\mathrm{m1}}} = \frac{5\ \mathrm{mV} \cdot 28\ \mu\mathrm{S}}{2 \cdot 25\ \mathrm{kHz} \cdot 15\ \mathrm{pF}} = 186\ \mathrm{mV}. \tag{5.7}$$

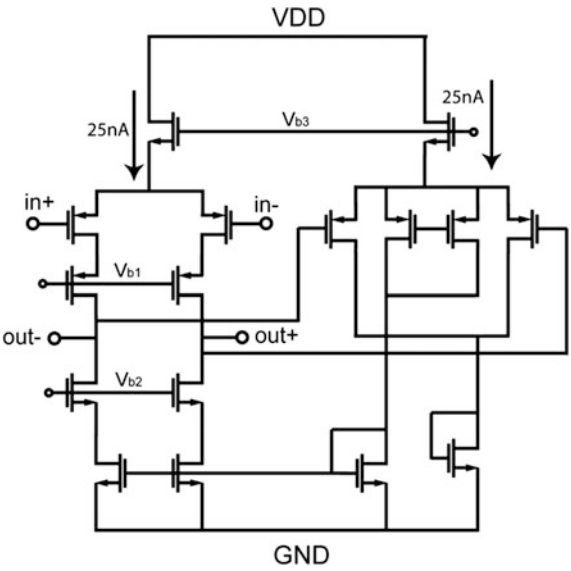

Fig. 5.9 Schematic of G_{m5}

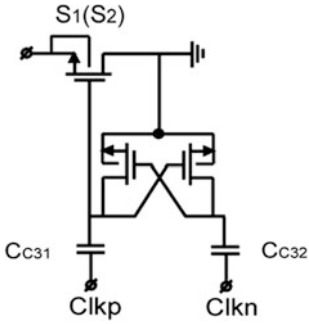

Fig. 5.10 Switch S_1 (S_2) in the RRL and its driving circuit

As a result, with F equal to 85 dB, the output-referred residual ripple should then be less than 17 μV, which is sufficient.

Several parasitic effects can generate residual ripple. First, the output of G_{m5} has to switch between its own offset and the voltage required to compensate for G_{m1}'s offset. Due to the finite driving capability of G_{m5}, the charging and discharging of the parasitic capacitances at its output will result in spikes that will finally turn into a residual ripple at the output of the CCOPA. To reduce this effect in a power efficient manner, the output swing of G_{m5} should be reduced. With an offset of G_{m1} equals to 5 mV and G_{m4}/G_{m1} equals to 1/22, the output voltage swing of the integrator is limited to 100 mV. Second, the charge injection and clock feed-through errors will result in a residual ripple as well. One obvious example is the parasitic capacitance C_{ps}, possibly due to layout, shown in Fig. 5.5. It introduces an AC error charge, which is directly coupled to the output of the CCIA. This residual ripple is at f_s, which is half of f_{chop}. To minimize this error, S_1 and S_2 are capacitively driven by a latch (Fig. 5.10), which limits their overdrive voltage to

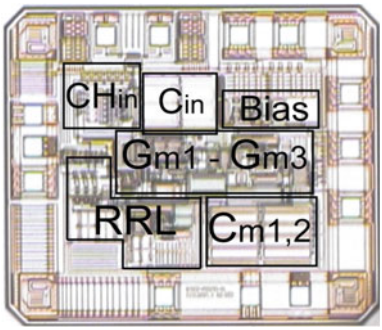

Fig. 5.11 Chip micrograph

about half of the VDD. Thus, the charge injection errors are also reduced by half. Moreover, symmetrical layout of all the switches is a must.

5.3.3 Experimental Results

The CCOPA was implemented in a HV 0.7 μm CMOS process (Fig. 5.11). It consumes 10 μA from a 5 V supply. Histograms of the residual ripple and the residual offset (at f_{chop} = 25 kHz) are shown in Fig. 5.12. Typical PSRR and CMRR are higher than 114 and 140 dB, respectively. Its CMVR (−0.6 to 20 V) is not limited by CH_{in} and C_{in}, but rather by the ESD protection diodes of the pads used. Its noise spectrum is shown in Fig. 5.13 with a 1/*f* noise corner at around 0.5 Hz.

The transfer function of the CCOPA is shown in Fig. 5.14, and a narrow notch at f_{chop} is observed. Step responses at different input CM voltages are shown in Fig. 5.15. It can be seen that the step response contains slowly decaying transient ripple. This is because the input choppers demodulate signals near f_{chop} to DC, where they are blocked by the input capacitors. This problem is exacerbated by the use of the RRL, since this acts as a notch filter. The net result is an amplifier whose step response exhibits slow-settling ripple at f_{chop}. This is a major drawback of this CCOPA.

At a gain of 20 and a 70 pF capacitive load, the CCOPA is stable. The input bias current is less than 400 pA, and the input offset current is less than 300 pA. Table 5.1 summarizes the CCOPA's performance and compares it to the state of the art. It can be seen that this is the only opamp that achieves a CMVR significantly higher than its own supply. Compared to the LV opamps, it achieves a much wider CMVR and a competitive NEF, and compared to a HV opamp, its power consumption is much lower due to the absence of a HV supply.

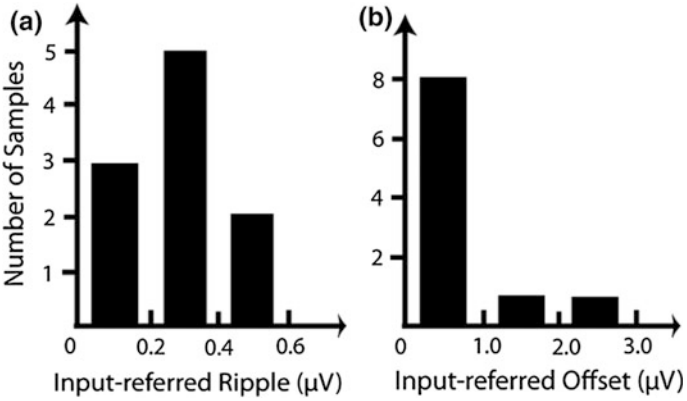

Fig. 5.12 Input-referred ripple @ gain = 100 (**a**) and offset (**b**), measured on 10 samples

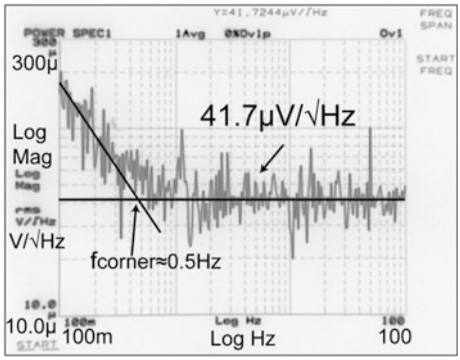

Fig. 5.13 Output noise spectrum density (gain = 1000)

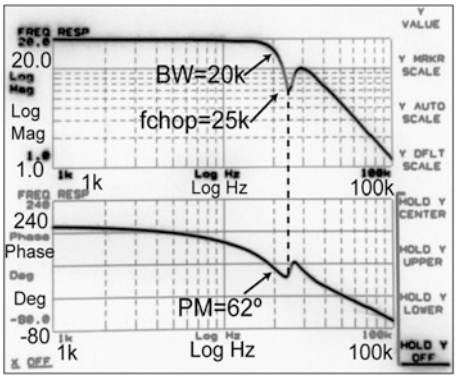

Fig. 5.14 Transfer function of the CCOPA (gain = 20)

Table 5.1 Comparison with state-of-the-art opamps

	This work	[12]	[13]	[14]	[15]	[16]
CMVR (V)	20 > *Vdd*	40 = *Vdd*	1.8 = *Vdd*	1.8 = *Vdd*	3 < *Vdd*	5 = *Vdd*
Power (W)	50 μ	7.2 m	30.6 μ	2.65 m	715 μ	72 μ
Offset (μV)	3	120	3	0.78	1	1.94
Noise (nV/$\sqrt{\text{Hz}}$)	42	5.1	55	5.9	10.5	37
NEF	5.1	8.3	8.7	8.4	4.8	5.4
GBW (kHz)	400 gain > 20	11,000	350	4000	1800	260 kHz gain > 10
GBW / I_{supply}	40	6.1	20.6	2.7	12.6	6.1

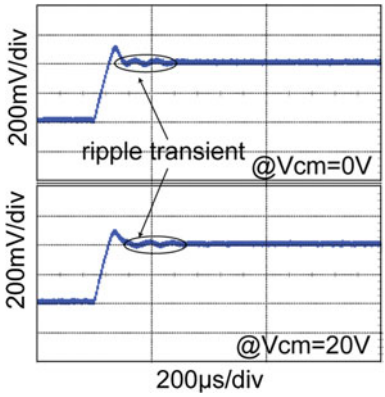

Fig. 5.15 Step response of the CCOPA at different input CM voltages with 70 pF load capacitor @ G = 20

5.4 Multipath CCOPA

In the previous section, a basic CCOPA has been described, which achieved wide input CMVR with high power efficiency and high precision. However, it has a transfer function notch around f_{chop}, which is a significant drawback. Moreover, its bandwidth should be limited such that the RRL notch is beyond the signal band. To solve these problems, a multipath capacitively-coupled chopper-stabilized operational amplifier (MCCOPA) is proposed. It employs an AC-coupled high-frequency path (HFP) which has high gain at the notch frequency, thus effectively "burying" the notch.

5.4.1 Design of the Multipath CCOPA (MCCOPA)

As shown in Fig. 5.16, the MCCOPA consists of an AC-coupled high-frequency path (HFP) and a chopped low-frequency path (LFP). The HFP consists of a

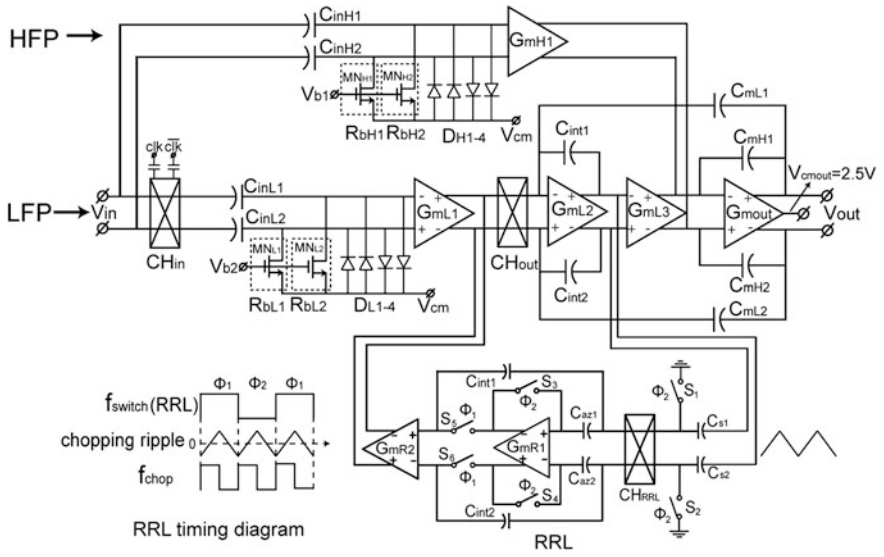

Fig. 5.16 Schematic of the MCCOPA

two-stage amplifier: an input stage G_{mH1} and a Miller integrator output stage built around G_{mout}. As in the basic CCOPA, the DC CM inputs are blocked by HV poly-poly capacitors C_{inH1} and C_{inH2} (8 pF), and so the input CM voltage of G_{mH1} can be set by two resistors $R_{bH1,2}$. $R_{bH1,2}$, which are implemented as NMOS transistors biased in the subthreshold region (Fig. 5.8) [10]. D_{H1}–D_{H4} are employed to protect G_{mH1} during large input CM transients. The HFP actually has a band-pass transfer function. The high-pass corner is theoretically determined by the time constant of $C_{inH1,2}$ and $R_{bH1,2}$: $f_{highpass} \frac{1}{2\pi R_{H1,2} C_{inH1,2}}$.

The LFP consists of a four-stage chopper amplifier: an input stage G_{mL1} (similar to G_{mH1}) an integrator built around G_{mL2}, a transconductor G_{mL3}, and an output stage G_{mout} (shared with the HFP). As in the HFP, DC CM signals are blocked by identical input capacitors $C_{inL1,2}$. However, DC differential signals are up-modulated by the input chopper CH_{in} and so can be amplified. As a result, the MCCOPA's low-frequency behavior is defined by the LFP.

To ensure a wide CMVR, the input chopper used in the basic CCOPA is again employed here, and to suppress the chopping ripple, the same SC RRL is also used. The rest of this section will discuss the amplifier's frequency compensation, noise, and residual offset.

5.4.1.1 Frequency Compensation

To smoothly combine the HFP and the LFP, multipath hybrid Miller compensation is employed [17], with $G_{mH1}/C_{mH1,2} = G_{mL1}/C_{mL1,2}$. The frequency at which the

gain of the HFP is equal to that of the LFP is called the crossover frequency f_{cross}. To obtain a smooth transfer function, the high-pass corner of the HFP should be lower than f_{cross}. Below the crossover frequency f_{cross}, the LFP dominates; while above it, the HFP takes over. f_{cross} can be tuned by adjusting $C_{\text{int1,2}}$ and G_{mL3}. For instance, reducing $C_{\text{int1,2}}$ reduces the bandwidth of the LFP, thus moving f_{cross} to a lower frequency. Reducing G_{mL3} also reduces the bandwidth of the LFP, but also decreases its DC gain. Thanks to the HFP, the LFP does not need to obtain a good phase margin around the −3 dB bandwidth of the MCCOPA.

5.4.1.2 Noise Considerations

To ensure that the MCCOPA has a flat noise floor, careful design is required, since there are several noise sources. The noise floor should be determined by thermal noise: that of G_{mL1} at low frequencies and that of G_{mH1} at high frequencies. To achieve this, f_{cross} should be set higher than the $1/f$ noise corner frequency of G_{mH1}, so that its $1/f$ noise can be suppressed by the LFP; while the $1/f$ noise of G_{mL1} is up-modulated and suppressed by the HFP. The biasing resistors $R_{\text{bH1,2}}$ and $R_{\text{bL1,2}}$ also contribute noise. The noise current of $R_{\text{bH1,2}}$ is integrated on $C_{\text{inH1,2}}$ and appears as extra low-frequency noise at the inputs of $G_{\text{mH1.}}$ When referred to the input of the HFP, this noise (V_{nRH}) can be calculated by:

$$V_{nRH} = \sqrt{4kT / R_{\text{bH1,2}}}\,\frac{1}{2\pi f\, C_{\text{inH1,2}}} \tag{5.8}$$

As a result, V_{nRH} becomes significant at low frequencies. Fortunately, this noise will be suppressed by the extra gain of the LFP. However, to ensure that this suppression is sufficient, $R_{\text{bH1,2}}$ must be carefully designed. At f_{cross}, V_{nRH} is calculated to be $\sqrt{4kT / R_{\text{bH1,2}}}\,\frac{1}{2\pi f_{\text{cross}} C_{\text{inH1,2}}}$, and $R_{\text{bH1,2}}$ should be made large enough to ensure that this noise is negligible compared to the desired noise floor of the whole MCCOPA. At lower frequencies, V_{nRH} increases, but the LFP also becomes more and more dominant. Thus, the net result is that the noise contribution of $R_{\text{bH1,2}}$ stays almost constant. At higher frequencies, V_{nRH} will decrease automatically.

The noise in the LFP also needs to be carefully designed. The noise current of $R_{\text{bL1,2}}$ is again integrated by $C_{\text{inL1,2}}$ and appears to be significant at low frequency. However, this excessive low-frequency noise is up-modulated to high frequency by chopping and thus is less significant in signal band. The DC noise contribution of $R_{\text{bL1,2}}$ can be calculated by Eq. (3.3).

5.4.1.3 Offset Considerations

Since the HFP is AC-coupled, its offset limits the residual offset of the entire MCCOPA. This is because the DC input of G_{mH1} is set to zero by the AC-coupling network, and so the HFP's offset will appear as an offset current at the output of

G_{mH1}. In the presence of a feedback network around the MCCOPA, this current will then be canceled by the LFP via G_{mL3}. The HFP's millivolt-level offset will thus be suppressed by the ratio of the combined DC gain of G_{mL1}, G_{mL2}, and G_{mL3} on the one hand, and the DC gain of G_{mH1} on the other. Meanwhile, the offset of the LFP itself is largely eliminated by chopping.

5.4.2 Implementation of the Multipath CCOPA

The implementation details of the input chopper, the SC RRL, are the same as those of the basic CCOPA; thus, they will not be repeated here. The frequency compensation of the MCCOPA, and the implementation of its HFP and the LFP will be presented in the following.

5.4.2.1 Frequency Compensation

As mentioned earlier, merging the HFP and the LFP smoothly is critical in the design of the multipath CCOPA. For this purpose, hybrid Miller compensation is employed which requires $G_{mH1}/C_{mH1} = G_{mL1,2}/C_{mL1,2}$. With $G_{mH1,2} = G_{mL1,2} = 14\ \mu S$, $C_{mH1,2}$ and $C_{mL1,2}$ are chosen to be 3 pF so that a *GBW* of 743 kHz is set. The crossover frequency f_{cross} is set just above the $1/f$ noise corner of G_{mL1} (~ 5 kHz). The high-pass corner of the HFP, however, must be designed lower than f_{cross}. The theoretical high-pass corner of the HFP is determined by $C_{inH1,2}$ and $R_{bH1,2}$. With $C_{inH1,2} = 8$ pF and $R_{bH1,2} = 500\ M\Omega$, it is 40 Hz, which is much lower than f_{cross}. The choice of $R_{bH1,2}$ is based on noise considerations and will be explained in the following.

5.4.2.2 Implementation of the HFP

The HFP is a classic two-stage Miller compensated amplifier. Its input pair is biased in weak inversion to achieve high noise efficiency. With $G_{mH1} = 14\ \mu S$, its white noise floor is around 50 nV/$\sqrt{\text{Hz}}$.

The output stage must obtain good driving capability. As a result, G_{mH2} employs a class-AB output stage, which is the same as that of the single-path CCOPA introduced above. The schematic of the HFP is shown in Fig. 5.17.

As explained before, $R_{bH1,2}$ can generate excessive low-frequency noise and thus must be carefully designed. In this work, $R_{bH1,2}$ are chosen to be 500 MΩ, so that at f_{cross}, its noise contribution [calculated by Eq. (5.8)] is roughly 22 nV/$\sqrt{\text{Hz}}$. This is not significant compared to the noise of G_{m1} (50 nV/$\sqrt{\text{Hz}}$). As frequency goes lower, the noise calculated by Eq. (5.8) increases, but it will be suppressed by the increasing gain of the LFP. The result is a more or less constant noise contribution in the entire bandwidth.

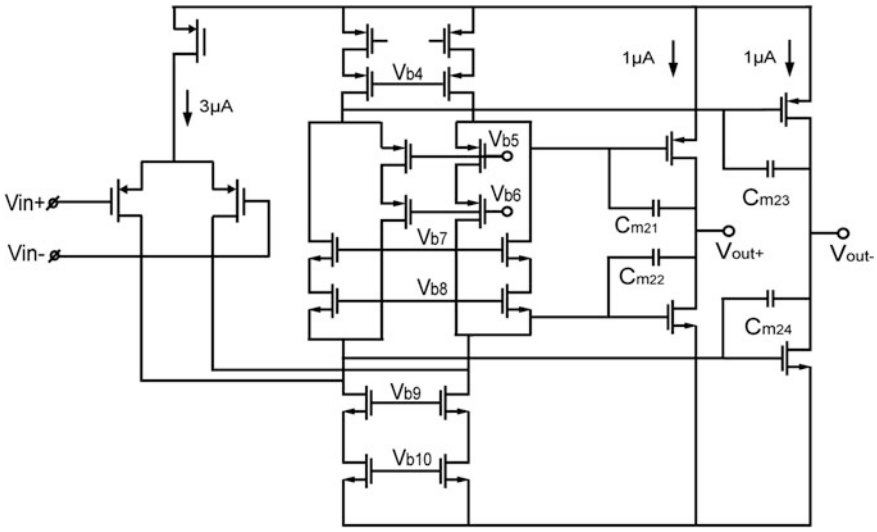

Fig. 5.17 Schematic of the HFP

5.4.2.3 Implementation of the LFP

The LFP determines the low-frequency performance such as residual offset and low-frequency noise floor. To obtain a minimum noise floor, the input stage G_{mL1} is biased in weak inversion, whose noise floor is also 50 nV/$\sqrt{\text{Hz}}$. Its topology is the same as G_{mH1} in the single-path CCOPA (Fig. 5.7).

To suppress the offset of the HFP, the LFP must obtain sufficient DC gain. Moreover, it should not have a very wide bandwidth. This is not only for power saving, but also to suppress the residual ripple generated in the LFP due to chopping. As a result, an integrator built around G_{mL2} is used to increase the DC gain of the LFP and simultaneously suppress the chopping ripple. G_{mL2} employs a classic folded-cascode amplifier, which offers $\sim$80 dB DC gain. A compensation transconductance G_{mL3} is also often chosen to be relatively small to limit the bandwidth of the LFP. Moreover, it must provide sufficient current to compensate for the offset current of G_{mH1}. As a result, it is often designed as a differential pair biased in strong inversion. The tail current is determined by the maximum expected offset current of G_{mH1}. In this case, a maximum 5 mV offset from G_{mH1} is expected, which requires 70 nA compensating current. Thus, the tail current source of G_{mL3} is chosen to be 90 nA.

Like $R_{bH1,2}$, $R_{bL1,2}$ must be carefully designed to minimize its noise contribution. Its input-referred noise contribution can be calculated by Eq. (3.3). With f_{chop} chosen to be 50 kHz and $R_{bL1,2}$ = 50 MΩ, its input-referred noise contribution is 7.2 nV/$\sqrt{\text{Hz}}$, which is negligible compared to the noise of G_{mL1}.

With a total open-loop DC gain of 200 dB, the LFP can sufficiently suppress the offset of the HFP. The residual offset V_{resoff} can be estimated as follows:

$$V_{\text{resoff}} = V_{\text{oH}} \frac{A_{\text{Gm1}} \times A_{\text{Gm2}}}{A_{\text{LFP}}}, \tag{5.10}$$

where V_{oH} is the offset of G_{mH1} and is estimated as 5 mV. With $A_{Gm1} \times A_{Gm2} \approx 120$ dB, the residual offset is expected to be no bigger than 0.5 μV

5.4.3 *Experimental Results of the MCCOPA*

The multipath CCOPA was realized in a HV 0.7 μm CMOS process and has an active chip area of 1.35 mm^2 (Fig. 5.18). It has an input CM range of 20 V, which is limited by the ESD diode of the input bond pads and draws only 8 μA from a 5 V supply. Measurements on 14 samples show that its input offset is less than 3 μV (Fig. 5.19a). The multipath CCOPA's DC PSRR is greater than 120 dB, while its DC CMRR is greater than 148 dB (Fig. 5.19b). The input-referred noise density is 56 nV/$\sqrt{\text{Hz}}$, which is flat until at least 100 MHz (Fig. 5.20a). The input offset current is below 95 pA, and the input bias current is less than 107 pA.

With resistive feedback, the residual ripple was measured at a closed-loop gain of 100. Only the residual ripple at f_{chop} is significant, which has an input-referred mean amplitude of 0.125 μV and a maximum of 0.28 μV.

The frequency response of the multipath CCOPA is shown in Fig. 5.20b, where no significant notch is observed. Differential step responses at 0 and 20 V DC input CM voltages are shown in Fig. 5.21a. Figure 5.21b shows the transient output ripple during step response with (above) and without (below) the multipath architecture, respectively. It is obvious that the multipath architecture greatly suppresses the transient output ripple. Moreover, there are no output spikes as observed in [18]. The CM step response of the multipath CCOPA is shown in Fig. 5.21c. During a large descending CM step, MN_{11-22} are shortly turned on at the moment when their drain voltages reach V_{ref}–0.7 V. This greatly speeds up the settling

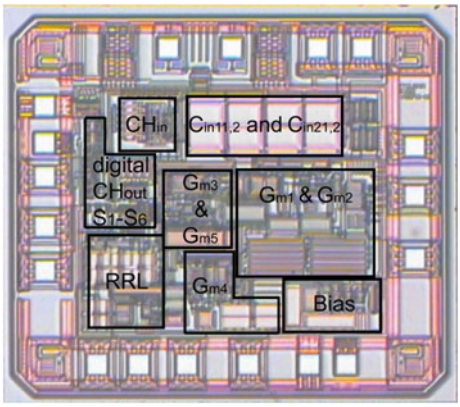

Fig. 5.18 Chip micrograph

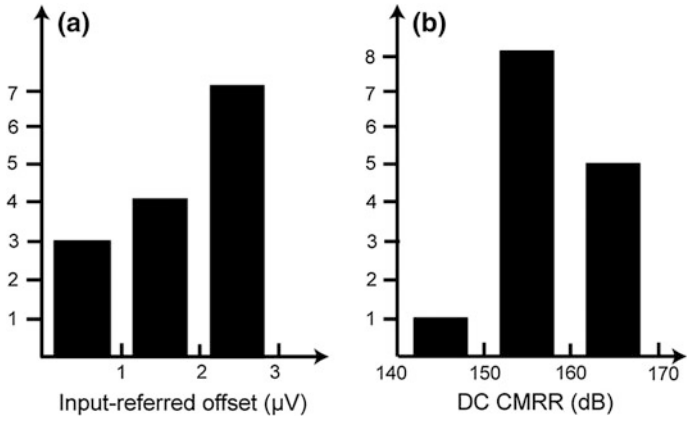

Fig. 5.19 Input-referred ripple (**a**) and offset (**b**), measured on 10 samples

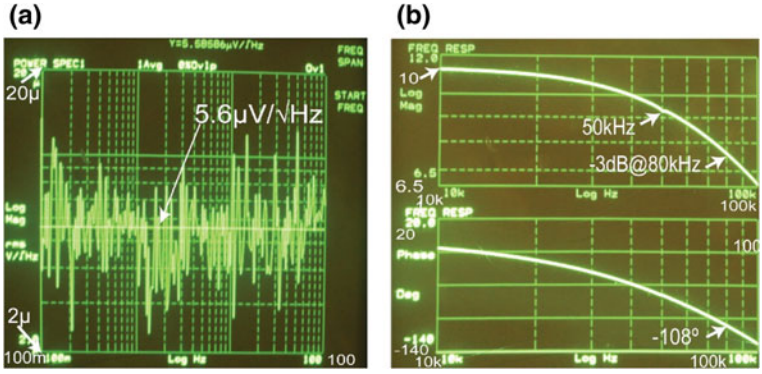

Fig. 5.20 Output noise spectrum density (gain = 1000) (**a**); notch in the transfer function of the CCOPA (gain = 20) (**b**)

process. The multipath CCOPA has a GBW of 800 kHz and is stable at a gain of 20 with 50 pF capacitive load. In Table 5.2, the multipath CCOPA's performance is summarized and compared with the state of the art. Compared to a classic rail-to-rail opamp [5], it is able to achieve a CMVR far above its supply. Compared to a HV opamp [4], it does not require HV supply and thus saves significant power consumption. Compared to a single-path CCOPA, the step response of a multipath CCOPA exhibits much less ripple, which also decays much faster. It also achieves 2 × more bandwidth.

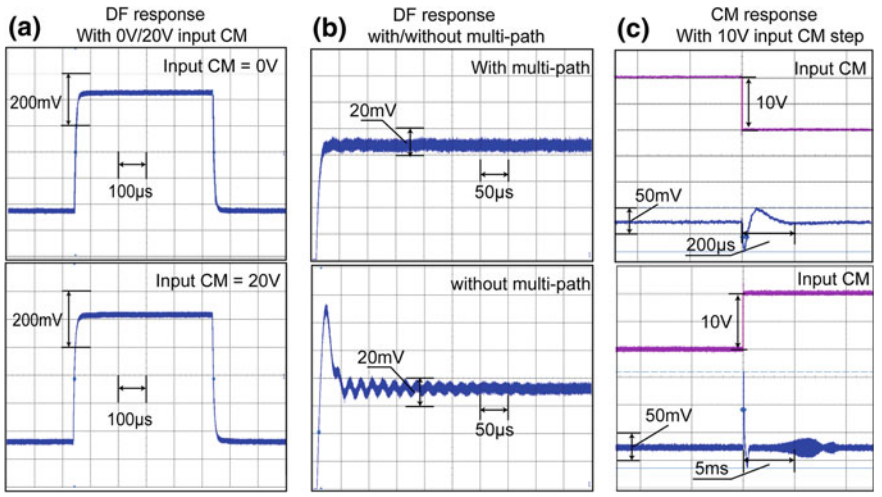

Fig. 5.21 Step response of the CCOPA at different input CM voltages with 70 pF load capacitor @ G = 20 (**a**); chip photo (**b**)

Table 5.2 Comparison with state-of-the-art opamps

	MCCOPA	Single-path CCOPA	[4]	[5]	[6]	[7]	[9]
CMVR (V)	20 > *Vdd*	20 > *Vdd*	40 = *Vdd*	1.8 = *Vdd*	1.8 = *Vdd*	3 < *Vdd*	5 = *Vdd*
Power (W)	40 µ	50 µ	7.2 m	30.6 µ	2.65 m	715 µ	72 µ
Offset (µV)	3	3	120	3	0.78	1	1.94
Noise (nV/√Hz)	56	42	5.1	55	5.9	10.5	37
NEF	6.1	5.1	8.3	8.7	8.4	4.8	5.4
GBW (kHz)	800 gain > 20	400 gain > 20	11,000	350	4000	1800	260 kHz gain > 10
GBW / I_{supply}	100	40	6.1	20.6	2.7	12.6	6.1

5.5 Conclusions

Two CCOPAs have been described and implemented. Both opamps feature wide input CMVR, high power efficiency, and high DC precision. However, the single-path CCOPA has a simple architecture and suffers from a notch in the transfer function. This notch results in a slowly decaying ripple during a step response. To overcome this problem, the multipath CCOPA can be used. The AC-coupled HFP buries the notch, and consequently, a much smoother step response is obtained. Both CCOPAs achieves 3 µV input-referred offset more than 140 dB DC CMRR and good NEF of 5.1 and 6.1, respectively.

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Chapter 6
Capacitively Coupled Chopper Instrumentation Amplifiers for High-Side Current Sensing

In Chap. 1, it was mentioned that high-side current sensing is an important application for capacitively coupled chopper amplifiers. In this chapter, capacitively coupled chopper instrumentation amplifiers (CCIA) for this particular application will be introduced in detail.

In Sect. 6.1, the background of current sensing is briefly introduced. Section 6.2 gives an overview of existing state-of-the-art IAs intended for this application. This is followed by the system level design of the proposed CCIA in Sect. 6.3. The realization details of the CCIA will be presented in Sect. 6.4. Experimental results will be given in Sect. 6.5 and the chapter ends with conclusions.

6.1 Introduction

In power management systems, the supply current of a battery is often monitored by a small series resistor R_{sense} which converts the current into a voltage V_{sense} (Fig. 1.1). To minimize the power consumption of R_{sense}, V_{sense} must be minimized. However, the CM level of V_{sense} is quite high—nearly as high as the battery voltage. Thus, IAs with low offset and low $1/f$ noise as well as with high DC CMRR are required. Since it is capable of meeting all these requirements, the CCIA is a good candidate for this application.

In practice, the sensing resistor R_{sense} can also be placed between the load R_{load} and the ground. However, this method cannot detect an accidental short between the supply and the ground. Moreover, some systems cannot tolerate ground disturbances due to the voltage drop across R_{sense} especially in the presence of a high load current [1]. As a result, high-side current sensing is usually preferred, despite its difficulties.

Q. Fan et al., *Capacitively-Coupled Chopper Amplifiers*,
Analog Circuits and Signal Processing, DOI 10.1007/978-3-319-47391-8_6

6.2 Overview of the State of the Art

6.2.1 HV Chopper-Stabilized Current Feedback Instrumentation Amplifier

In 2008, a chopper-stabilized current feedback instrumentation amplifier (CFIA) for high-side current sensing was published by Witte [2]. A simplified block diagram of this amplifier is shown in Fig. 6.1. The chopper stabilization technique introduced in Sect. 2.2.2 was adopted, resulting in the use of two signal paths: a high-frequency path (HFP) (G_{m21}, G_{m22}, and G_{m5}) and a low-frequency path (LFP) (G_{m11}, G_{m12}, G_{m3}, G_{m4} and G_{m5}). Each path, in turn, consisted of a CFIA (HFP: G_{m21}, G_{m22}, G_{m5}; LFP: G_{m11}, G_{m12}, G_{m3}, G_{m4} and G_{m5}). The gain of the CFIA is $\frac{G_{m11}(G_{m21})}{G_{m12}(G_{m22})} \times \frac{R_1+R_2+R_3}{R_2}$, where G_{m11}/G_{m12} defines the low-frequency gain, while G_{m21}/G_{m22} determines the high-frequency gain. For better matching and hence high gain accuracy, G_{m11} was made equal to G_{m12}, as were G_{m21} and G_{m22}. The high-gain LFP suppressed the offset of the HFP, while its own offset was removed by chopping. In this way, the IA achieved microvolt offset and low $1/f$ noise, as well as a high CMRR. To suppress the chopping ripple, G_{m11} and G_{m12} were auto-zeroed, as explained in Sect. 2.3.5. To expand the CMVR, G_{m21} and G_{m11} were implemented with HV DMOS transistors that were powered from the input CM voltage (30 V). However, this resulted in increased power consumption. Moreover, good layout alone was not enough to reduce the mismatch between the input and feedback transconductors to levels commensurate with the target gain accuracy of 0.1 %, and thus each transconductor was degenerated by trimmed resistors. A consequence of this was a further increase in noise and power consumption. In total, the IA consumed 9 mW of power, which is quite significant.

6.2.2 HV Current-Mode Three-Opamp Instrumentation Amplifier

In 2009, a current-mode chopper IA based on the three-opamp topology was published by Schaffer [3]. A simplified block diagram of this IA is shown in Fig. 6.2. It consisted of two input buffers, which increased the input impedance and converted the input voltage into current. This current was then mirrored by the two sets of current mirrors and then converted into an output voltage by $R_{1,2}$. Each stage in Fig. 6.2 again employed a multipath chopper-stabilized topology, as shown in Fig. 6.3. With chopping, this IA achieved microvolt offset, low $1/f$ noise, and a high CMRR. Unlike the topology shown in Fig. 6.1, G_{min} (Fig. 6.3) was not auto-zeroed. Thus, a notch filter was employed to suppress the chopping ripple, as explained in Sect. 2.3.1. To increase the input CMVR, the input buffers were

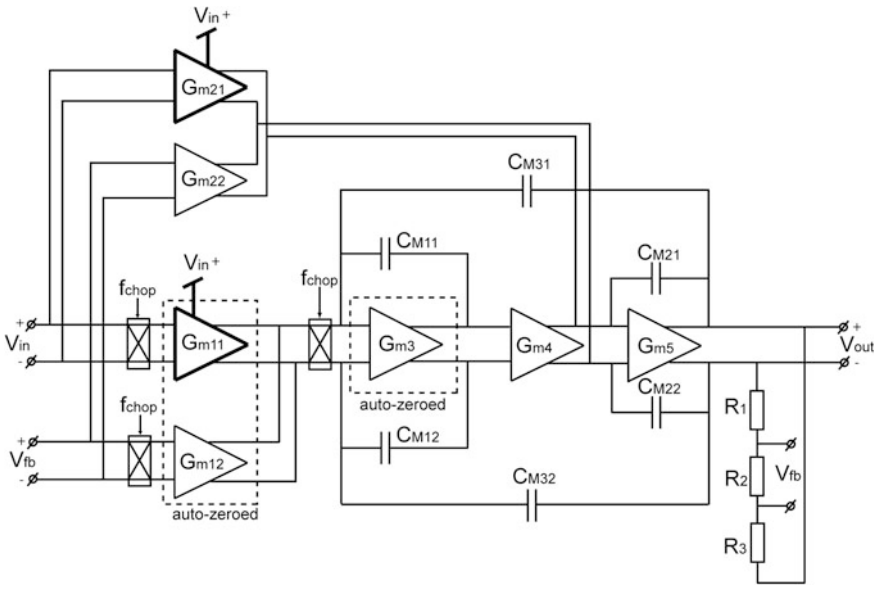

Fig. 6.1 Simplified block diagram of a chopper-stabilized CFIA for high-side current sensing (transconductors in *bold* were implemented with HV transistors)

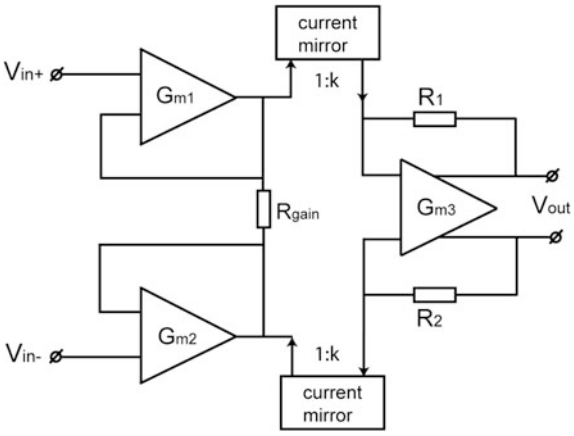

Fig. 6.2 Simplified block diagram of a current-mode three-opamp-based IA for HV applications

powered from an HV supply which consumed 21 × more power (79 mW) than the IA's LV part. Moreover, since the CMVR of a three-opamp IA cannot include the rail, this HV supply had to be larger than the intended input CM voltage.

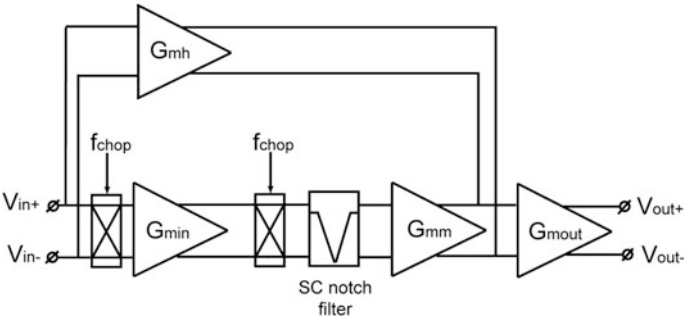

Fig. 6.3 Block diagram of the topology used in $G_{m1}/G_{m2}/G_{m3}$

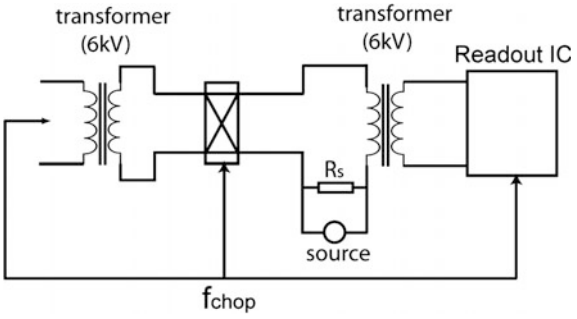

Fig. 6.4 Simplified block diagram of an HV IA with an on-chip microtransformer

6.2.3 HV IA with Isolated Transformer

An isolated transformer-based IA was published in 2010 by Rothan [5] (Fig. 6.4). In this design, an on-chip transformer isolated the CM input voltage. As a result, the CMVR was extended to 6 kV. Due to the CM isolation provided by the transformers, the readout IC could be implemented by LV transistors. However, the design was still very power-hungry. To ensure a reasonable transformer size, the signal was up-modulated to a high frequency (20 MHz), thus requiring the readout IC to have at least the same bandwidth. This eventually led to a 15.6 mW power consumption, even with a 1.2 V supply.

6.2.4 Conclusions

In the above state-of-the-art designs, a wide CMVR was achieved at the cost of considerable power consumption. A CCIA, however, offers both a wide CMVR and a high power efficiency and is thus should perform better in current-sensing applications.

6.3 Design of the CCIA for Current-Sensing Applications

The proposed CCIA is shown in Fig. 6.5 and consists of a floating input chopper (CH_{in}), input capacitors ($C_{in1,2}$), a feedback chopper (CH_{fb}) and feedback capacitors ($C_{fb1,2}$), an output chopper (CH_{out}), and a CCIA opamp. The CCIA opamp consists of an input stage G_{m1} and a nested-Miller integrator built around G_{m2} and G_{m3}. To first order, the gain of the CCIA is $C_{in1,2}/C_{fb1,2}$ as explained in Sect. 3.2. The DC CM level of G_{m1} is fixed by biasing resistors $R_{b1,2}$. Like the design presented in Chap. 5, the input transistors of G_{m1} must be protected from large input CM voltage steps by four diodes connected in parallel with $R_{b1,2}$ (Fig. 6.5). To expand the CMVR, poly-on-poly capacitors ($C_{in1,2}$ and $C_{fb1,2}$) with a 30 V breakdown voltage and high linearity (3 ppm) are employed. Thus, any circuitry behind the input capacitors $C_{in1,2}$ can be implemented by LV components. Compared to [2], the use of an LV input differential pair, instead of the HV counterpart which normally exhibits lower transconductance at the same biasing current, confers better performance such as lower input-referred noise with the same biasing current. To suppress the chopping ripple, a ripple-reduction loop (RRL) is applied. Unlike the RRL presented in Sect. 5.3.2, a different realization of a continuous-time (CT) RRL will be explored in this design.

The rest of the section will focus on the design of the input floating chopper, the RRL, and the opamps (G_{m1}, G_{m2} and G_{m3}) of the CCIA.

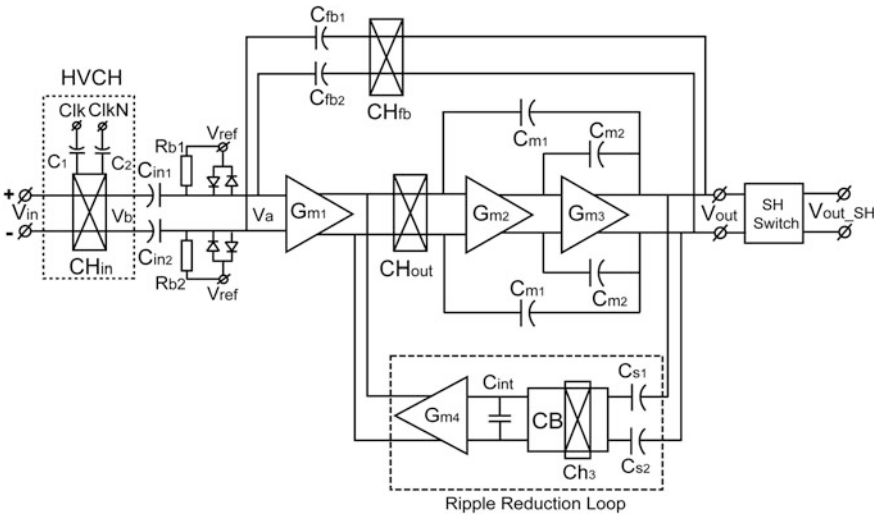

Fig. 6.5 Schematic of the CCIA for current-sensing application

6.3.1 Input Chopper

In Chap. 4, three choppers with a beyond-the-rail CMVR were proposed: a floating chopper driven by a single latch for signals smaller than 300 mV (Fig. 4.7); a floating chopper driven by a double latch for signals smaller than 300 mV (Fig. 4.8); and a floating chopper driven by a single latch for relatively large signals (~ 1 V) (Fig. 4.9). Thus, the most suitable solution must be chosen. In current-sensing applications, the signal amplitude is often smaller than 100 mV, and thus, the choppers shown in Figs. 4.7 and 4.8 are sufficient. Moreover, the source impedance of a current-sensing amplifier is often in the range of hundreds of milliohm to hundreds of ohm; thus, the errors due to the asymmetry of the input chopper become negligible. As a result, the simplest floating chopper (Fig. 4.7) was chosen for this application.

6.3.2 Ripple-Reduction Loop (RRL)

Since the CCIA is chopped, the up-modulated offset and $1/f$ noise of G_{m1} will cause output ripple which should be suppressed by an RRL. In this design, the RRL employed (Fig. 6.5) is different from the one presented in Chap. 5, which was first described by Wu in 2009 [7]. Later in Sect. 6.5, a comparison between this realization and the switched-capacitor RRL presented in Chap. 5 will be made.

First, sense capacitors $C_{s1,2}$ convert the ripple voltage into an AC current, which is demodulated by Ch_3 and then integrated into C_{int} via a current buffer (CB). G_{m4} converts the integrated voltage into a DC current, which cancels the offset of G_{m1}, and thus cancels the ripple. As explained in Sect. 2.3, the RRL creates a notch which suppresses the AC component of the amplifier's output signal at f_{chop}. A systematic analysis of the RRL, including the depth and the width of the notch, can be found in [7].

However, the analysis given in [7] is based on an active integrator; thus, a very brief analysis of the passive integrator-based RRL will be given in the following. First, the RRL is cut open at the output of G_{m4} (Fig. 6.6). The loop gain of the RRL can then be obtained from the ratio between the output current of G_{m4}, I_{com} and the offset current of G_{m1}, I_{offset}. Due to I_{offset}, a ripple will be present at the output of the CCIA. There are two possible signal paths for the ripple current: via C_{m1}, or via G_{m2} and C_{m2}. Since the ripple is a relatively high-frequency signal, it will follow the high-frequency path (C_{m1}). For simplicity, we will assume that the ripple is integrated into a triangular waveform, and its amplitude (peak-to-peak) at the output of G_{m3} is given by $\left|V_{ripple}\right| \approx \frac{I_{offset}}{2 \times f_{chop} \times C_{m1}}$. This ripple will be converted into an AC current by C_s. The amplitude of this current (I_{ripple}) is given by:

$$\left|I_{ripple}\right| = \left|V_{ripple}\right| \times 2C_s \times f_{chop}. \tag{6.1}$$

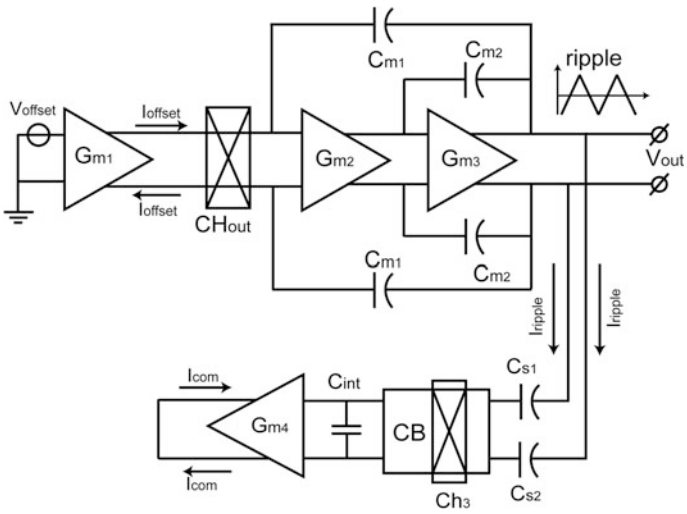

Fig. 6.6 Schematic of the RRL for ripple suppression factor analysis

I_{ripple} is then demodulated to DC by Ch_3. The amplitude of the DC current is equal to that given by Eq. (6.1). The output voltage of CB $V_{\text{CB\_out}}$ then equals:

$$V_{CB\_\text{out}} = \left|I_{\text{ripple}}\right| \times R_{CB}, \tag{6.2}$$

where R_{CB} is the output impedance of CB. If Eqs. (6.1) and (6.2) are combined, the current at the output of G_{m4} (I_{com}) can be given by:

$$I_{\text{com}} = \frac{I_{\text{offset}}}{C_{m1}} \times R_{CB} \times C_s \times G_{\text{m4}}. \tag{6.3}$$

Thus, the ripple suppression factor F, or the loop gain of the RRL, is given by:

$$F = \frac{I_{\text{com}}}{I_{\text{offset}}} = \frac{R_{CB} \times C_s \times G_{\text{m4}}}{C_{\text{m1}}}. \tag{6.4}$$

It can be seen that to increase F, the DC output impedance of the CB must be increased. Moreover, increasing G_{m4} should also help. However, as the impedance cannot be too high, since it is also used to limit the noise of the RRL, it is usually chosen to be much smaller than G_{m1}, as explained in Chap. 5. Decreasing C_{m1} helps to increase F, but it also increases the original ripple amplitude. Increasing C_s seems to be the most favorable way to increase F, but a closer look at an actual implementation shows that R_{CB} is also related to C_{s} therefore canceling the effect of varying C_{s}. This will be revisited later in Sect. 6.4 with the help of a detailed circuit schematic.

6.3.3 CCIA Opamp

Ideally, the CCIA's opamp is the only active block that consumes significant amounts of DC supply current. Thus, the CCIA's power efficiency is highly determined by the design of this opamp. To achieve high power efficiency, the input differential pair of G_{m1} (Fig. 6.5) should be biased in weak inversion. Although this is a simple and straightforward approach, it cannot easily be done in a CFIA [2] due to the large CM-dependent mismatch between the input and feedback transconductances. However, due to the CM-blocking effect of the input capacitors, it can be easily done in a CCIA.

To guarantee enough loop gain, three gain stages are employed (Fig. 6.5). Thus, nested-Miller compensation is employed [4]. To ensure stability, the same Miller compensation scheme explained in Sect. 5.3.1 is used. Compared to the conventional nested-Miller compensation, where the dominant pole is determined by G_{m1} and C_{m1}, the dominant pole of this CCIA is determined by G_{m2} and C_{m2}. The purpose of doing so is to avoid the use of a large C_{m1}, since G_{m1} is usually very large to achieve low noise.

To ensure good driving capability, a class-AB output stage is employed. Further implementation details such as the dimension of critical components and the full opamp schematics will be given in Sect. 6.4.

6.3.4 Output Spikes

As discussed in Chap. 3, a CCIA produces output spikes when an output voltage V_{out} is present. Since the feedback capacitors $C_{fb1,2}$ have to be charged and discharged to either $+V_{out}$ or $-V_{out}$ in every clock cycle, the output stage must supply this current instantly. Due to the finite output impedance and the limited current capacity, spikes are generated. However, in current-sensing applications, an ADC is often employed after the preamplifier. Thus, with proper timing, the ADC only samples the CCIA's output when it has settled. To showcase this possibility, a sample-and-hold (S&H) switch together with two hold capacitors ($C_{H1,2}$) are employed at the output of the CCIA. The timing diagram is shown in Fig. 6.7. The

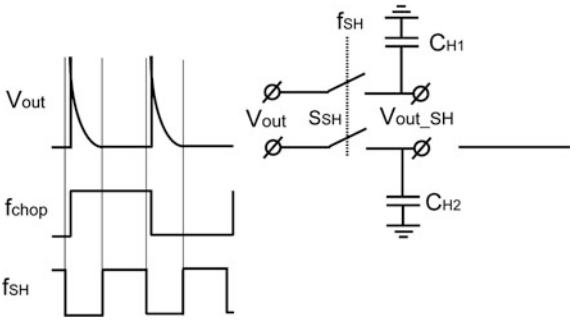

Fig. 6.7 Timing diagram of the sample-and-hold (S&H) switch

duty cycle of the S&H clock can be customized with regard to the width of the spikes. With the S&H switch, the CCIA can also be used as a stand-alone IA, provided that it does not have to drive heavy loads.

6.4 Realization

In this section, implementation details of the CCIA are given. First, the design of the global parameters including the chopping frequency and the capacitor network is given. Then, the critical dimensions of the input chopper and CM biasing circuit, along with important design parameters of the RRL and the CCIA opamp, will be presented.

6.4.1 Global Parameters (Chopping Frequency and Capacitor Bridge)

The choice of the chopping frequency (f_{chop}) is not straightforward because several factors must be taken into account. First, f_{chop} should be far away from the signal bandwidth, since the RRL will result in a notch in the CCIA's transfer function around f_{chop}. Thus, in this case, f_{chop} should be at least higher than 1 kHz. Second, f_{chop} should be higher than the $1/f$ noise corner of the CCIA, so as to fully remove the $1/f$ noise from the signal band. Third, the residual offset depends on the charge injection and clock feed-through errors of the chopper switches as explained in Sect. 2.4. Thus, a relatively slow f_{chop} is preferred to achieve the lowest possible residual offset, especially for technologies with a relatively large feature size (consequently more parasitics) and poorer matching. A fourth consideration is the residual ripple, which is due to chopping. Although the RRL suppresses the ripple, its circuit non-idealities still result in a residual ripple. This residual ripple at f_{chop} or the harmonics of f_{chop}, as will be explained in detail in Sect. 6.4.5, may only be filtered by the integrators in the CCIA. Thus, with low f_{chop}, these errors will become significant. Based on these considerations, f_{chop} is chosen to be 50 kHz in this work. Later, measurement results will prove that this choice results in a good combination with both low residual offset and low residual ripple.

The design of the capacitor network involves several considerations. First, since the gain accuracy of the CCIA depends on the matching between $C_{in1,2}$ and $C_{fb1,2}$, their capacitance should be relatively large. However, from the cost point of view, these capacitors should be as small as possible to save chip area. In this work, $C_{in1,2}$ is chosen to be 4 pF and for a gain of 20, $C_{fb1,2}$ is thus 200 fF, which results in about 0.1–0.2 % mismatch. It should be pointed out that the bottom plates of $C_{in1,2}$ and $C_{fb1,2}$ should be connected to the input and the output, respectively, rather than the virtual ground of the CCIA, as shown in Fig. (6.5). This is because the

excessive parasitic capacitance associated with the bottom plates will increase the noise of the CCIA according to Eq. (3.10).

With f_{chop} = 50 kHz and $C_{in1,2}$ = 4 pF, the input impedance of the CCIA is theoretically 2.5 MΩ, which is sufficient for the current-sensing application.

6.4.2 Implementation of the Input Chopper

As explained in Chap. 4, the input floating chopper is implemented by HV floating NMOS transistors. The on-resistance of these transistors must be low enough to ensure that their noise is much lower than the input-referred noise of the CCIA's opamp. In this design, the noise of the CCIA's opamp is set to around 30 nV/√Hz so that the total noise voltage of the CCIA in the signal band (1 kHz) is around 1 μV, which is comparable to the targeted residual offset (a few microvolts). Thus, the on-resistance of the chopper switches is designed to be around 1 kΩ, which generates only 4 nV/√Hz noise and, thus, is completely negligible. To achieve this on-resistance, switches with a W/L = 6/0.7 μm are employed which are driven by 2 V clock signals. This low overdrive voltage helps to reduce the clock feed-through error, especially in the presence of a parasitic capacitance, from the gate to the source/drain of the chopper switches due to layout. This clock signal is realized by using 0.1 pF coupling capacitors (C_{11} and C_{12}) with around 50 fF total parasitic capacitances at the gate of a chopper switch transistor, which is in accordance with Eq. (6.1). The minimum sizes of the latch transistors and the model circuit are chosen to reduce charge injection and clock feed-through errors. The resistors to limit the current spikes are chosen to be 50 kΩ. A smaller resistance will result in more current spikes, while a larger resistance will occupy more chip area and lead to a slower transient response due to the larger RC time constant formed at the input of the chopper.

6.4.3 Implementation of the CM Biasing Circuit

The biasing resistor can be implemented in several ways. The simplest approach is to use an on-chip resistor. However, to ensure that the noise of the CCIA is dominated by the noise of the CCIA's opamp (30 nV/√Hz), the noise generated by $R_{b1/2}$ should not be more than 15 nV/√Hz. With f_{chop} = 50 kHz and C_{in} = 4 pF, $R_{b1,2}$ should be at least 50 MΩ, according to Eq. (3.3). Too much chip area would be taken up with on-chip resistors. An alternative is to use MOS transistors biased in the subthreshold region [8], as shown in Fig. 6.8b. MN_1 is biased by MN_2, which is connected in diode fashion. The W/L (60/10) ratio of MN_2 is much larger than that of MN_1 (1.5/10), so that the output resistance of MN_1 is sufficiently large and can thus be used to implement the biasing resistor. The resistance, however, is highly nonlinear with process spread, corner, and temperature. More importantly, it

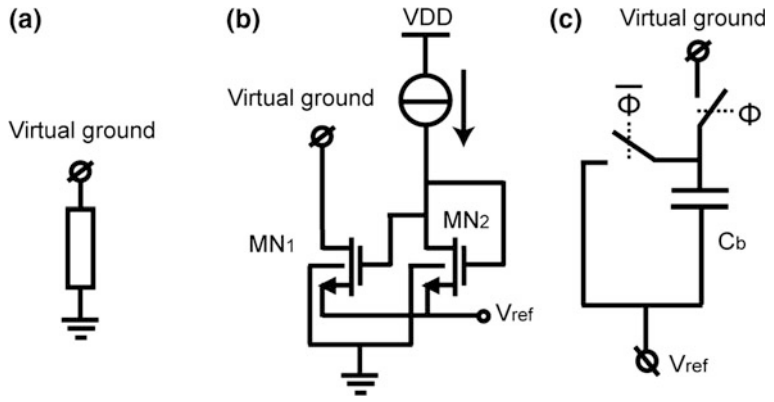

Fig. 6.8 Schematic of **a** the biasing resistor implemented with an on-chip resistor; **b** NMOS in the subthreshold region; **c** and with a switch-capacitor circuit

is highly dependent on the drain–source voltage of MN_1. This has a dramatic influence on the CM settling of the CCIA. In particular after a CM step transient, the virtual ground is charged to either *V*ref + 0.7 V or *V*ref − 0.7 V. In the first case, the output resistance of MN_1 will significantly increase, which results in a much slower settling time calculated by Eq. (3.5); in the second case, MN_1 will be turned on, dramatically reducing the time constant. The latter can be considered an advantage. To take advantage of this effect also in the first case, two biasing resistors implemented with PMOS transistors can also be added, which will then be turned on to reduce the settling time drastically.

To overcome the nonlinear settling behavior and large process spread while saving chip area, an SC biasing circuit can be used, which is shown in Fig. 6.8c. It forms an equivalent resistor between the virtual ground of the CCIA and V_{ref}. This resistance can be calculated as $\frac{1}{C_b \times f_S}$, where f_S is the switching frequency. Theoretically, there are an infinite number of combinations of C_b and f_s which would result in a 50 MΩ equivalent resistance. However, to prevent the virtual ground of the CCIA from drifting away slowly, f_S should not be too slow. Moreover, C_b should be smaller than $C_{in1,2}$; otherwise, it will increase the equivalent parasitic capacitance at the input of G_{m1}, which in turn will increase the input-referred noise of G_{m1}, according to Eq. (3.7). Nevertheless, it should not be so small as to increase the equivalent biasing resistance, which in turn leads to a long settling time. In this work, f_S is chosen to be equal to f_{chop}, and C_b is chosen to be 1 pF. This results in a CM settling time of 200 µs. With an SC biasing circuit, the presence of parasitic capacitances can lead to residual errors. Consider a mismatched parasitic capacitance C_p between the clock line and the signal line as shown in Fig. 6.9a which is possibly due to layout. A net AC current I_{cp} is injected into the virtual ground. If f_s is synchronized with f_{chop}, I_{cp} is also synchronized with f_{chop} as shown in the timing diagram of Fig. 6.9b. This error must be compensated by an AC current I_{cin}. To generate I_{cin}, a square wave at V_b is required which is also

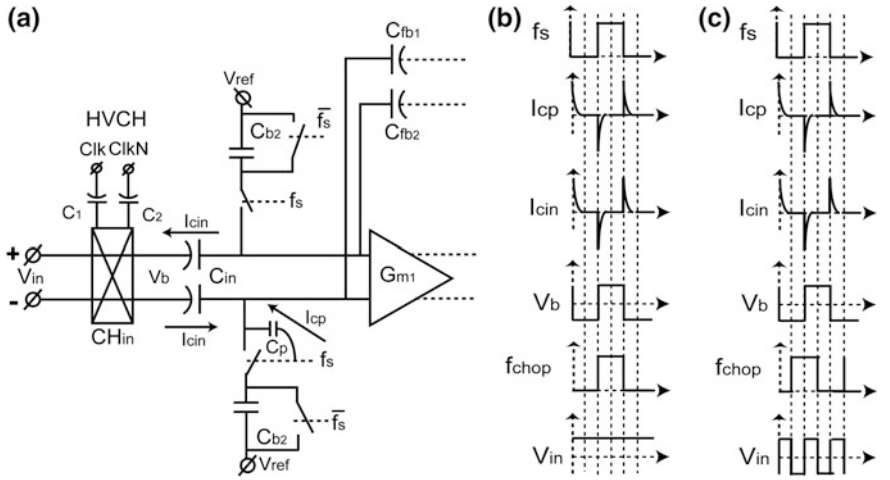

Fig. 6.9 **a** Schematic with the parasitic capacitance (C_p) associated with the SC biasing circuit; **b** timing diagram when f_s is synchronized with f_{chop}; **c** timing diagram when f_s is 90-degree phase shifted with regard to f_{chop} with f_{chop}

synchronized with f_{chop} (Fig. 6.9b). This consequently requires an equivalent input DC offset $V_{off,}$ which can be estimated by:

$$V_{off} = \frac{Q_{mis}}{2 \times C_{in}} = \frac{V_{clk} \times C_p}{2 \times C_{in}}, \tag{6.5}$$

where Q_{mis} is the net charge injected into the virtual ground node due to C_p. With C_{in} = 4 pF and V_{clk} = 3 V, a 1 fF C_p would result in a 375 μV input-referred offset. This is highly undesirable. To avoid this problem, f_s is chosen to be 90-degree phase shifted with regard to f_{chop}. A timing diagram of this situation is shown in Fig. 6.9c. In order to generate I_{cin} to compensate for I_{cp}, a square wave at V_b is required which is synchronized with f_s. Since f_s is 90-degree phase shifted with regard to f_{chop}, the result is an input-referred ripple at $2f_{chop}$, rather than an input-referred offset. This ripple can then be filtered by the integrator built around G_{m3}. Table 6.1 compares the three biasing methods. It can be seen that the resistor offers a clean, linear solution (free from clock spikes), but this solution could be

Table 6.1 Summary of the three biasing schemes

	Resistor	MOS in subthreshold	Switched-cap
Area	Large	Small	Small
Residual error	NA	NA	Ripple-offset
Linearity	High	Low	High
Accuracy	Medium	Low	Medium

impractical due to its large chip area. The transistors in the subthreshold offer area-efficient clean biasing, but they exhibit nonlinear behavior during large CM transients and suffer from wide process spread. SC biasing, on the other hand, provides an area-efficient linear solution, but can produce residual ripple due to the layout parasitic. In this design, the second and third biasing methods have been implemented and can be turned on and off separately. The residual ripple introduced by the SC biasing scheme is minimized by careful layout.

6.4.4 *Implementation of the CCIA Opamp*

A block diagram of the CCIA opamp is shown in Fig. 6.5. It consists of three stages. To achieve high power efficiency, the input stage of G_{m1} is biased in weak inversion. A schematic of the input stage is shown in Fig. 6.10. With an 8 μA bias current, G_{m1} is 70 μS. The input-referred noise of G_{m1} is around 30 nV/$\sqrt{\text{Hz}}$. The second-stage G_{m2} is used to provide more loop gain and to suppress the errors of the third stage. It employs a folded-cascode topology and is shown in Fig. 6.11. The third-stage G_{m3} employs a class-AB output stage to drive the feedback network and the load. Its schematic is shown in Fig. 6.11. Compared to its class-A counterpart, the class-AB output stage helps to sharpen the output spikes since it can provide a much larger transient current than its quiescent current. This helps to charge the feedback capacitors quickly during clock transients.

With three gain stages, nested-Miller compensation is employed to ensure stability, as explained in Sect. 6.3.4. Similar to the design presented in Chap. 5, to increase power efficiency, the pole at the output of G_{m2} is designed to be the dominant pole, and thus can be small to save power (20 μS), according to Eq. (5.2).

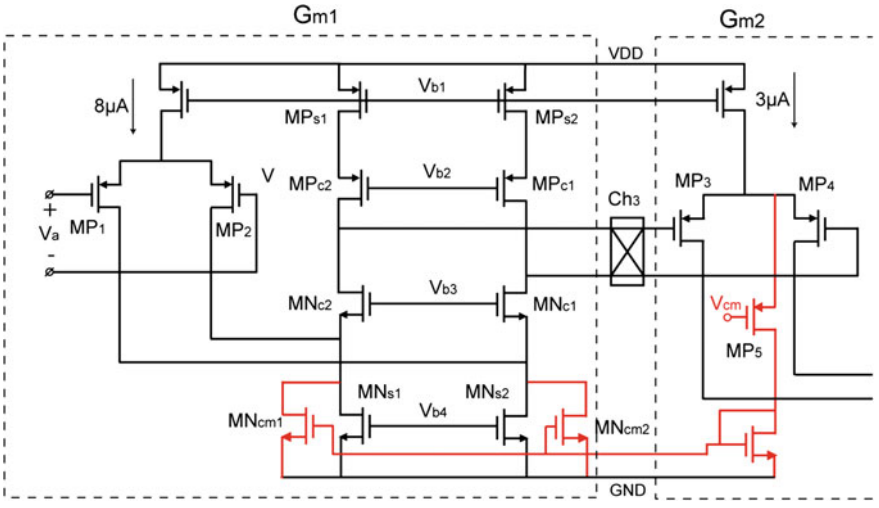

Fig. 6.10 Schematic of the input stage G_{m1}

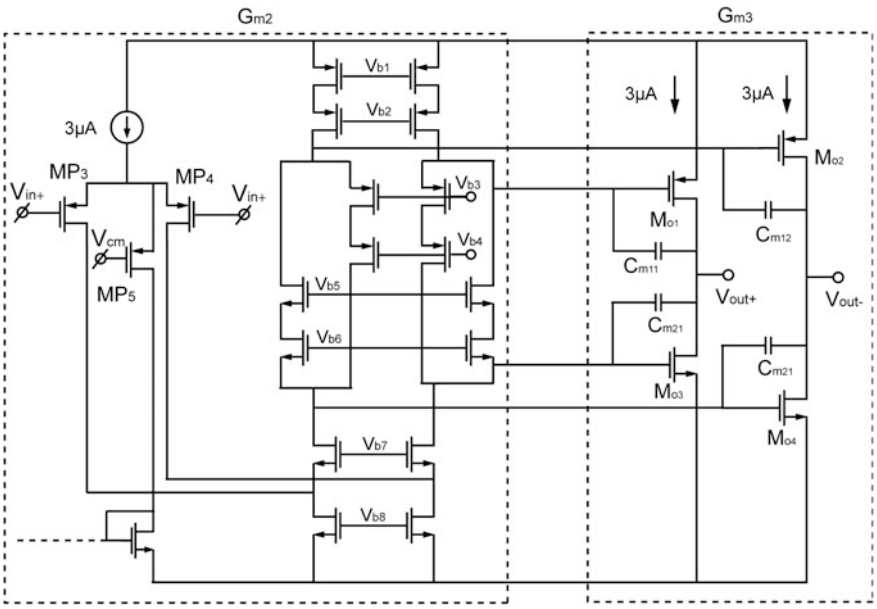

Fig. 6.11 Schematic of the second-stage G_{m2} and the output class-AB stage

G_{m3} is designed to be 70 μS to drive a maximum 40 pF capacitive load, and C_{m1} and C_{m2} are 4.3 pF. With a closed-loop gain of 20, Eq. (5.2) is thus satisfied:

$$\frac{20 \times 70\,\mu}{2\pi 40p} \geq \frac{2 \times 70\,\mu}{2\pi 4.3p} \geq \frac{4 \times 20\,\mu}{2\pi 4.3p} \tag{6.6}$$

Although chopping and RRL eliminate most of the offsets and ripples, care must be taken to ensure low residual errors due to various circuit non-idealities of the CCIA's opamp. The offset of G_{m1} has been up-modulated by chopping. However, it is still useful to reduce the offset of G_{m1}, since this causes output ripple. Although the offset would be reduced by the RRL, a proportionally large residual ripple can be expected due to the limited loop gain of the RRL. Moreover, with a large offset, the RRL must produce more compensating current, which could result in a large G_{m4}. This in turn could lead to an increase in the noise contributed by the RRL integrator. In this work, the dimension of the input transistors of G_{m1} is chosen to be 400/1. This helps to restrict the offset. The offset of G_{m2} is suppressed by the gain of G_{m1} at the chopping frequency. Thus, the offset of G_{m2} must not be too high either.

In this work, input transistors with a W/L ratio of 300/1 ensure good matching. Besides these, extra care must be taken to minimize the effect of parasitic capacitances. This is illustrated in Fig. 6.12. First, parasitic capacitance C_{p1} at the output chopper CH_{out} introduces an AC clock feed-through error. This AC current requires an AC voltage at the input of G_{m1}. Thus, a residual offset must appear at the input of the CCIA. This residual offset V_{os1} can be estimated by [9]:

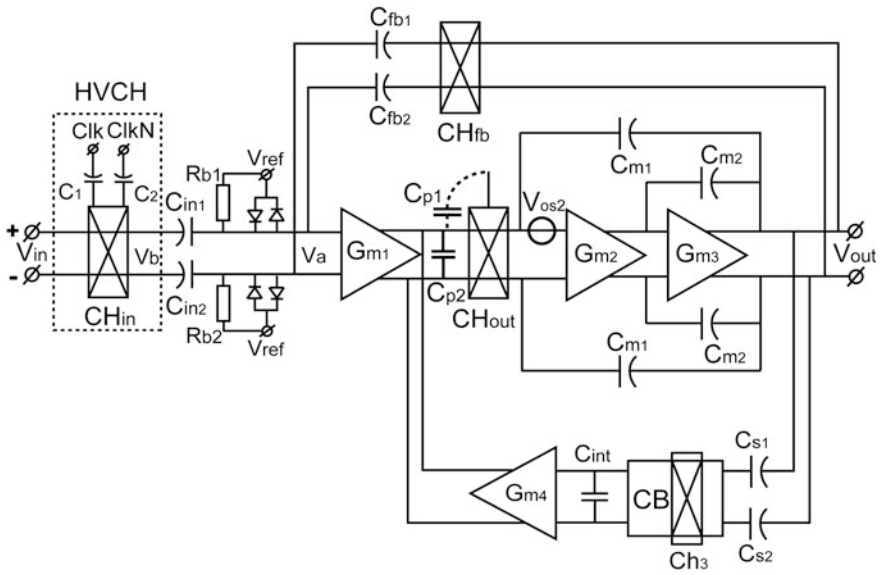

Fig. 6.12 Schematic of the CCIA opamp with critical parasitic capacitances

$$V_{os1} = \frac{2 \times V_{clk} \times f_{chop} \times C_{p1}}{G_{m1}}. \tag{6.7}$$

To reduce this error, the layout of CH_{out} must be as symmetrical as possible [9]. Secondly, the offset of G_{m2}, V_{os2}, is up-modulated by CH_{out}, forcing this AC voltage upon C_{p2}, which requests an AC current. This current again requires a residual offset at the input of the CCIA. This residual offset can be calculated by [9]:

$$V_{os1} = \frac{4V_{os2} \times f_{chop} \times C_{p2}}{G_{m1}}. \tag{6.8}$$

To reduce this effect, either the offset of G_{m2} or the parasitic capacitances C_{p2} must be minimized. In [10], efforts have been made to reduce the offset of G_{m2} with an extra offset reduction loop. In this work, attention has been paid to reduce the parasitic capacitances. As shown in Fig. 6.12, the critical parasitic capacitors are located at the input of CH_{out}. To minimize these, the dimension of the cascode transistors $MP_{c1,2}$ and $MN_{c1,2}$ has been minimized. Moreover, the input stage of the common-mode feedback (CMFB) circuit of G_{m1} has been moved to the output of CH_{out}. In this way, the parasitic capacitances can be kept within tens of femto-Farad. Thus, the resulting residual offset is negligible. In this case, the input stage of G_{m2} also functions as a part of the CMFB circuit. When the CM input voltage of G_{m2} becomes higher than V_{cm}, MP_5 draws more current, which is mirrored to $MN_{cm1,2}$. Since the current of $MP_{s1,2}$ stays unchanged, the drain–source voltage of $MN_{s1,2}$ must decrease. This in turn reduces the output CM voltage.

6.4.5 Implementation of the Output S&H Switch

A schematic of the S&H switches is shown in Fig. 6.13. The switches are capacitively driven by two latches. In this way, the overdrive voltage of each switch is constant regardless of the output voltage. This minimizes the charge injection and clock feed-through errors even in the presence of a large output signal. The hold time is chosen to be 1/8 of a chopping clock cycle, which is enough to cover the spike.

6.4.6 Implementation of the RRL

A block diagram of the RRL is shown in Fig. 6.5; the ripple suppression factor was calculated in Sect. 6.3. Clearly, to increase the ripple-reduction factor F, the DC output impedance of the CB must be increased. A schematic of a basic CB together with C_s and C_{int} is shown in Fig. 6.14a. With this implementation, the output impedance of CB R_{CB} can be estimated as:

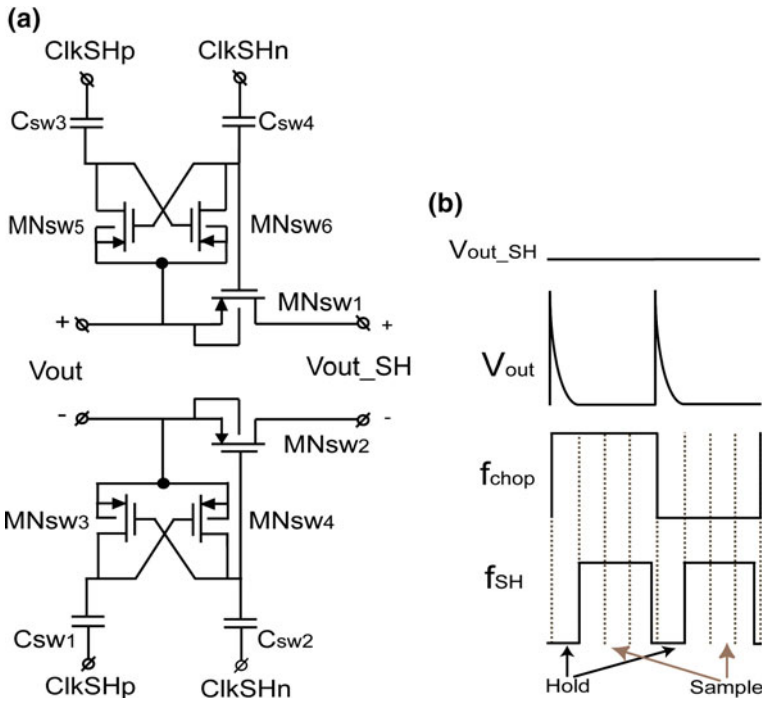

Fig. 6.13 Schematic of the S&H switch (**a**) and its timing diagram (**b**)

$$R_{\mathrm{CB}} = \frac{A}{2C_{\mathrm{s}} \times f_{\mathrm{chop}}}, \tag{6.9}$$

where A is the DC gain of the NMOS cascode transistors. Substituting Eq. (6.9) with Eq. (6.4) where $G_{\mathrm{m4}} = 4\ \mu\mathrm{S}$, $f_{\mathrm{chop}} = 50\ \mathrm{kHz}$, $A = 100$, and $C_{m1} = 4.3\ \mathrm{pF}$, F would equal 1300. Whether this suppression factor is enough or not depends on the uncompensated ripple. The uncompensated output ripple can be estimated by:

$$V_{\mathrm{ripple}} \approx \frac{V_{\mathrm{offset}} \times G_{\mathrm{m1}}}{2 \times f_{\mathrm{chop}} \times C_{m1}} = \frac{2\,\mathrm{mV} \times 70\,\mu S}{2 \times 50\,\mathrm{kHz} \times 4.3\,\mathrm{pF}} = 0.326\,\mathrm{V}, \tag{6.10}$$

where V_{offset} is the offset of G_{m1} and is estimated to be around 2 mV with W/L = 400/1 in this particular process. The resulting residual output ripple is about 250 μV, which may be too large for this application. Therefore, the suppression factor should still be increased by at least 10x. This can be easily achieved by employing two gain-boosting amplifiers around the cascode transistors (Fig. 6.14b). The effective gain of these cascode transistors is increased by the gain of the boosters. The boosters, however, have offset which introduces asymmetry into the CB and produces DC error output current. To overcome this problem, the boosters are chopped, as shown in Fig. 6.14b. This CB topology was first published by Kashmiri in 2009 [11].

Although gain-boosting increases the ripple suppression factor sufficiently, low residual ripple cannot be obtained without dealing with several circuit non-idealities and parasitic effects. First, the offset current of $MN_{1,2}$ and $MP_{1,2}$ is up-modulated,

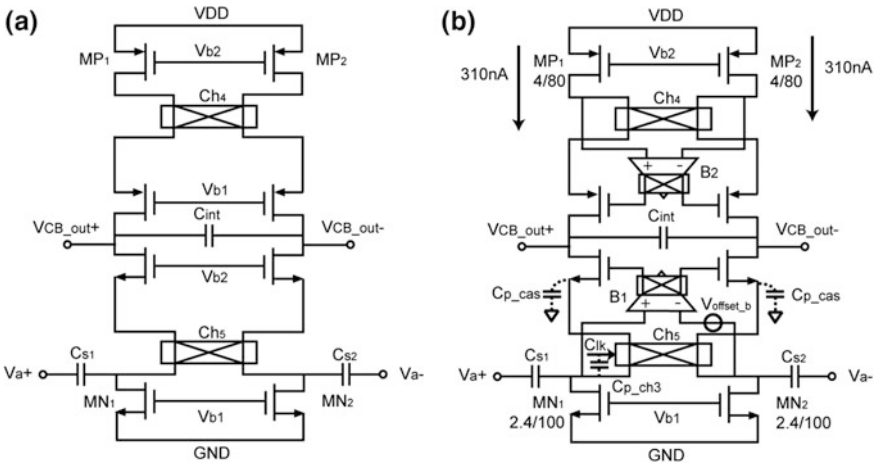

Fig. 6.14 Schematic of the basic CB (**a**) and the gain-boosted CB in the RRL (**b**)

which creates a triangular ripple at f_{chop} across C_{int}. The ripple amplitude V_{rip_1} can be calculated by:

$$V_{rip\_1} \approx \frac{I_{offset}}{2 \times f_{chop} \times C_{int}}, \tag{6.11}$$

where I_{offset} is the offset current of the current sources. This ripple can easily be hundreds of microvolts. It will be fed to the CCIA, up-modulated and finally turned into a second-harmonic ripple. To minimize this ripple, I_{offset} must be minimized. This can be done by choosing relatively large transistors to reduce the offset voltage, biasing the transistors in strong inversion, and decreasing the bias current to reduce its transconductance (Fig. 6.14b). A relatively large C_{int} is also employed (50 pF in this work). Second, the clock feed-through error introduced by the parasitic capacitance C_{p_ch3} shown in Fig. 6.14b can result in ripple which is directly coupled via C_s. This error V_{rip_2} can be estimated by:

$$V_{rip\_2} \approx \frac{V_{clk} \times C_{p\_ch3}}{C_s}. \tag{6.12}$$

If C_{p_ch3} is 1 fF, with C_S = 3 pF and V_{clk} = 3 V, V_{rip_3} is already 300 µV. Thus, the layout of Ch_3 is very critical and must be as symmetrical as possible.

Third, the offset of the gain boosters is up-modulated and appears at the sources of the cascode transistors. To charge and discharge the parasitic capacitors at these nodes, AC currents result which also create a ripple voltage across C_{int}. This ripple voltage V_{rip_3} can be calculated by:

$$V_{rip\_3} \approx \frac{V_{offset\_b} \times C_{p\_cas}}{C_{int}}, \tag{6.13}$$

where V_{offset_b} is the offset of the boosters. C_{p_cas} is the total parasitic capacitance at the sources of the cascode transistors. This ripple is then fed back to the CCIA opamp and up-modulated again by CH_{out}. The result is another second-harmonic ripple. To reduce this ripple, the parasitic capacitances at the sources of the cascode transistors should be minimized. In this design, the parasitic capacitors are kept at tens of femto-Farad; thus, this parasitic effect is negligible.

In total, the RRL consumes less than 6 µA, whereas the CB consumes 4 µA, and G_{m4} consumes 1 µA.

6.5 Experimental Results

The CCIA was realized in an HV 0.7 µm CMOS process and has an active chip area of 1.4 mm^2. The chip micrograph is shown in Fig. 6.15. It has an input CM range of ±30 V, while drawing 26 µA from a 3 to 5 V supply. Measurements with 12

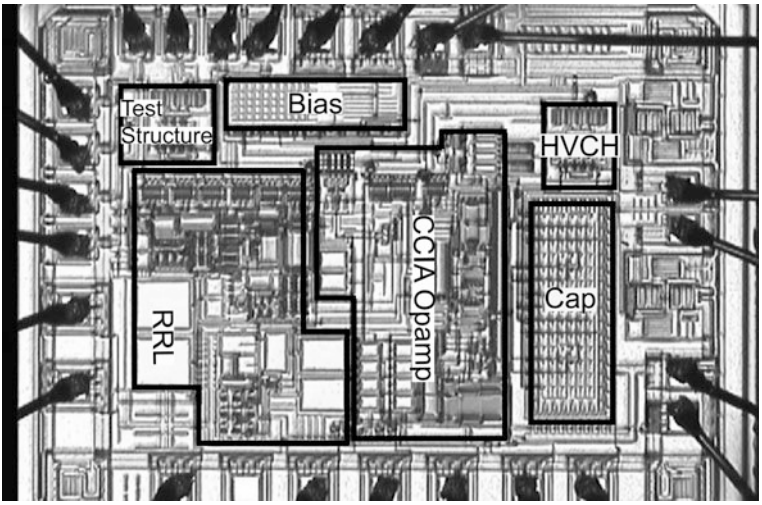

Fig. 6.15 Chip micrograph

samples show that its input offset is less than 5 μV (Fig. 6.16) with NMOS biasing, which increases by 0.25 μV with SC biasing. The DC PSRR of the CCIA is greater than 120 dB, while its DC CMRR is greater than 160 dB (Fig. 6.16), mainly because of the CM-independent drive voltages applied to CH_{in} and because the input capacitors isolate G_{m1} from CM voltage changes. The measured input-referred ripple at the chopping frequency (f_{ch} = 50 kHz) has a mean amplitude of 1.35 μV and a maximum of 3.9 μV with NMOS biasing, which translates into a 73 dB ripple-reduction factor. Compared to the SC RRL presented in Chap. 5, this RRL is

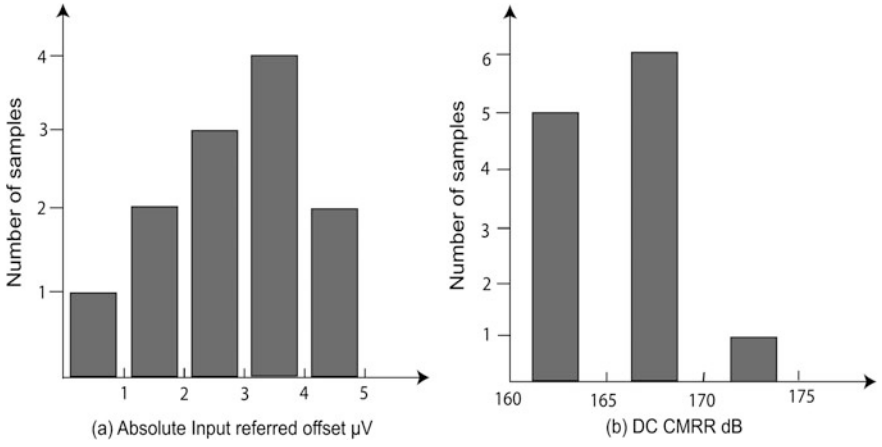

Fig. 6.16 Offset (**a**) and DC CMRR (**b**) histograms of the CCIA

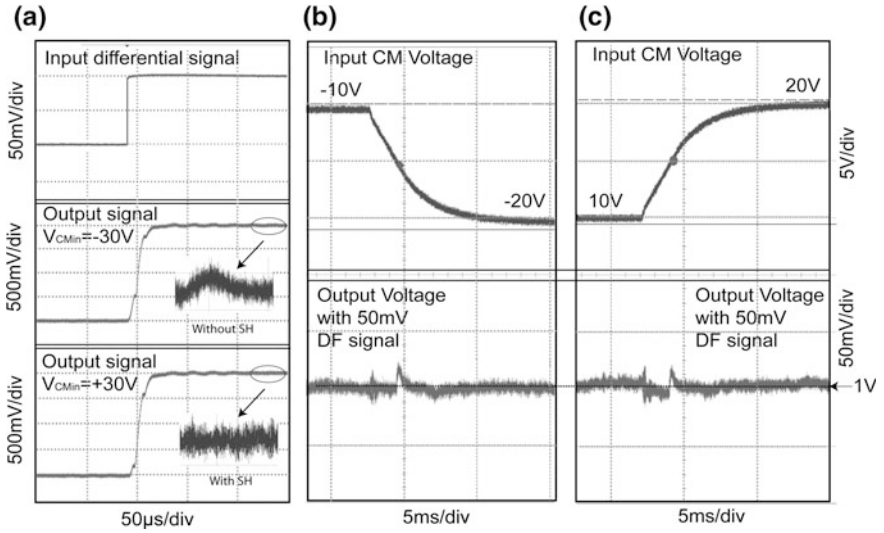

Fig. 6.17 Measured step response of the CCIA with a 100 mV differential DC input signal step at ±30 V CM voltage (**a**); with a 50 mV DC input signal and a 10 V negative CM step (**b**); with a 50 mV DC input signal and a 10 V positive CM step (**c**)

less area-efficient since the up-modulated offset of the current buffer CB must be well filtered by a relatively large integration capacitor C_{int} (50 pF) (Fig. 6.14), as mentioned in Sect. 6.4.5. The advantage, however, is that this approach suffers less from the charge injection and clock feed-through errors simply because it is a continuous-time solution and requires no switches other than those in the choppers. With SC biasing, the maximum ripple amplitude increases to 4 µV. Thanks to a good layout, the input-referred second-harmonic ripple is less than 8 µV with SC biasing. The input-referred noise density is 36 nV/$\sqrt{\text{Hz}}$ and 31 nV/$\sqrt{\text{Hz}}$, respectively, with and without the use of the output S&H switches. Step responses with a 100 mV differential signal at +30 and −30 V CM input voltages are shown in Fig. 6.17a. It can be seen that the S&H switches significantly suppress the output spikes. The amplifier's response to large positive and negative CM steps is shown in Fig. 6.17b, c. With a 40 pF capacitive load and the output S&H switches, the CCIA achieves a GBW of 1 MHz and a gain accuracy of 0.13 %. A frequency response of the CCIA is shown in Fig. 6.18.

In Table 6.2, the performance of the CCIA is summarized and compared with the state of the art. Its DC CM current draw is negligible, as it mainly consists of the leakage current of Dp_1 and Dp_2, which is less than 3 nA (430 pA with the chopper clock on) within the ±30 V CM range. Also, its differential input impedance is 1.6 MΩ, which is sufficient for current-sensing applications. Finally, it achieves the best NEF and GBW/I_{supply} factor among the listed state of the art.

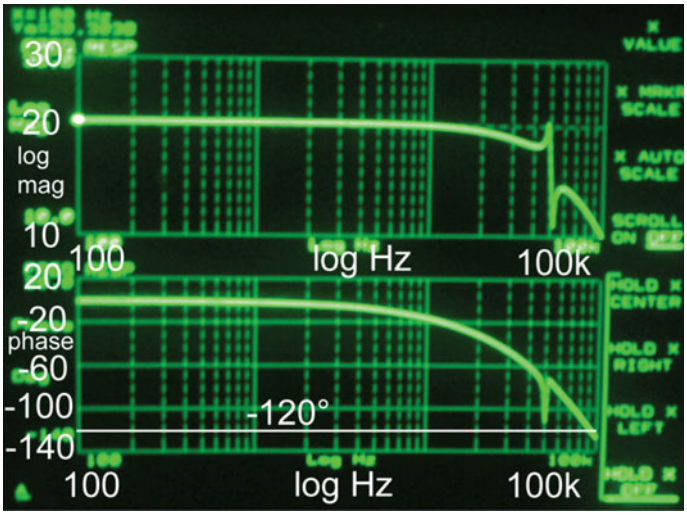

Fig. 6.18 Measured frequency response of the CCIA with a gain of 20 and 40 pF capacitive load

Table 6.2 Comparison of the proposed CCIA with several state-of-the-art designs

	This work	[2]	[3]	[12]
Technology	0.7 μm CMOS	0.8 μm BiCMOS	0.35 μm CMOS	
CMVR	−30 to +30 V	1.9–30 V	10–60 V	−20 to +75 V
Input DF range	±150 mV	±150 mV	±20 mV to ±1 V	±50 mV
Input offset (μV)	5	5	20	400
DC CMRR (dB)	160	143	120	80
DC PSRR(dB)	120	121	123	103
HVDC power	90 nW	6 mW	79.2 mW	>5 mW
	VHDD = 3	VHDD = 30	VHDD = 36	
LVDC power	78 μW	3.25 mW	3.75 mW	
	VLDD = 3	VLDD = 5	VLDD = 5	
Input noise (nV/$\sqrt{\text{Hz}}$)	31	136	19	60
Gain accuracy (%)	0.13	0.1	0.058	0.6
GBW (MHz)	1	1	8	6.75

6.6 Conclusions

A CCIA has been implemented for high-side current sensing. Due to the use of capacitive coupling at its input, the DC CM input currents are eliminated. No active blocks need to be powered by the HV supply, which saves considerable power

consumption compared to many other state-of-the-art designs [2, 3, 12]. With the proposed floating input chopper, the input CMVR is ±30 V, which is the breakdown voltage of the input high-voltage capacitors. Chopping helps to obtain low offset and low 1/*f* noise. Moreover, the chopping ripple is suppressed effectively by an RRL. The CCIA achieves a significant power reduction compared to IAs employing other topologies. At the same time, it obtains a competitive microvolt-level offset, high PSRR and CMRR, and good gain accuracy.

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Chapter 7
Capacitively Coupled Chopper Instrumentation Amplifiers for Low-Voltage Applications

Chapter 6 has explored the use of a CCIA for high-side current sensing applications, where its wide CMVR and high power efficiency can be optimally leveraged. In Low-voltage (LV) applications, despite the much smaller CMVR, these advantages, together with the CCIA's high gain accuracy, are still quite useful. Therefore, in this chapter, a CCIA for LV applications, e.g., sensor readout, will be presented.

This chapter starts with an introduction in which the targeted applications and requirements for the proposed CCIA are presented. Section 7.2 provides a brief overview of the state of the art, which is followed by the design of the proposed CCIA in Sect. 7.3. Section 7.4 discusses critical implementation details. Experimental results will be given in Sect. 7.5. Conclusions will be drawn in Sect. 7.6.

7.1 Introduction

One major application of LV precision IAs is in sensor readout. A first class of sensors, e.g., thermocouples and strain gauges, output small signals with bandwidths ranging from DC up to a few hundreds of Hertz, [1]. To accurately acquire such signals, precision IAs with microvolt offset and low 1/*f* noise are required. The CM level of such signals depends on the sensor's biasing condition and may vary from 0 V to the supply of the readout IC. Thus, a rail-to-rail CMVR is desired. A second class of sensors is used to acquire biomedical signals, e.g., the electrodes of ECG (electrocardiography) systems. Unlike the first class of sensors, such electrodes output small AC signals (tens of microvolts to a few millivolts) over bandwidths ranging from subHertz to hundreds of Hertz [1]. Normally, two electrodes are used to extract a differential signal. Due to the mismatch between the two electrochemical skin-electrode interfaces, a DC offset voltage (in the order of tens to hundreds of millivolts) is expected. Thus, the readout IA must suppress this "electrode offset" while amplifying the AC signals of interest. This requires a

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band-pass transfer function with a high-pass corner lower than 1 Hz. In the rest of the chapter, for simplicity, the first class of sensors will be referred to as DC sensors while the second class will be referred to as AC (biomedical) sensors.

Up to now, many state-of-the-art designs have been designed specifically to meet the requirements of one class of sensor. The proposed CCIA [2], however, aims to meet the requirements of both classes with the help of a minor reconfiguration which can be done at the PCB level. This minimizes the required hardware and facilitates its use in a cost-effective, general purpose readout system. Such a readout system can be used to monitor not only the health of patients (ECG and EEG), but also the environment around them, with the help of sensors that detect ambient temperature, humidity, etc.

To go one step further, the system can be converted into a wireless sensor node, as shown in Fig. 7.1. It consists of a sensor (a resistive bridge in this case), a readout IA, an ADC, a DSP unit, and an RF front-end to transmit the signal to the outside world. A wireless sensor node is typically powered by energy harvesters or by batteries and so should consume ultra-low power ($\ll$1 mW). It must also occupy a very small die area. These two specifications facilitate the cost-effective deployment of tens or even thousands of such nodes in medical diagnostics, and in heating, ventilation, and air conditioning (HVAC) systems [3–5].

As stated above, to be employed in such a sensor node, the CCIA should consume minimum power (a few micro-watts) and occupy a small chip area ($\ll$1 mm^2). Moreover, to save cost, the whole wireless sensor node should be eventually integrated on one die. Since the RF front-end is usually the most power-hungry block in a node, its efficient implementation determines the choice of the technology in which the entire node is realized. In practice, this means the use of deep submicron CMOS processes, as these result in RF front-ends with the least amount of area and the greatest power efficiency [6–8], while also being favorable for the implementation of ADCs and digital circuitry [9–11]. As a result, for full integration, the CCIA must then be realized in the same technology. Table 7.1 summarizes the requirements for the proposed CCIA, which has two modes: a DC mode for DC sensors (thermocouples, resistive bridges) and an AC mode for

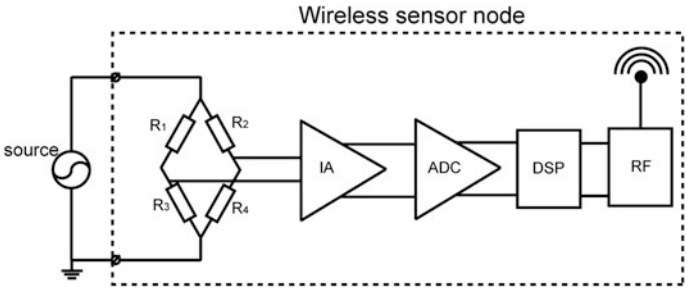

Fig. 7.1 Simplified block diagram of a wireless sensor node

Table 7.1 Requirements of the CCIA for wireless sensor nodes

	DC mode	AC mode
Offset	A few microvolts	N/A
Band-pass	N/A	0.5 Hz–100 Hz
Power (μW)	<10	<10
Area (mm^2)	≪1	≪1
CMVR	0 V−V_{DD}	0 V−V_{DD}
CMRR (up to 50 Hz) (dB)	>100	>100
Technology	Deep submicron	Deep submicron
Input impedance	High (>10 M ohm)	High (>10 M ohm)
Gain	100	100

biomedical sensors. It must meet both requirements and will be implemented in a standard 65 nm CMOS technology.

In the following section, several state-of-the-art designs for both DC and AC measurements will be briefly introduced. After that the design of the multi-purpose CCIA will be given.

7.2 Overview of the State of the Art

As most precision IAs are intended for either DC or AC measurements, the overview of the state of the art is divided into two parts: one about DC-sensing IAs and the other about AC-sensing IAs.

7.2.1 State-of-the-Art Precision IAs for DC Sensing

A number of state-of-the-art precision IAs can be found in the literature [12–15]. They feature low offset and 1/*f* noise, and a high DC CMRR and PSRR, which are essential for measuring small signal DC sensors. Recently, the current feedback topology has become very popular due to its high CMRR, input impedance, and the easily obtained rail sensing capability (either ground or supply). Thus, it is shown as an example in the following section.

7.2.1.1 A Current Feedback Instrumentation Amplifier (CFIA)

A recently published CFIA for sensor readout is shown in Fig. 7.2 [12]. It employs the chopper stabilization technique to achieve low offset and consists of two signal paths: a high-frequency path (HFP) and a low-frequency path (LFP). Each signal path consists of a CFIA. The LFP suppresses the offset of the HFP with its sufficient

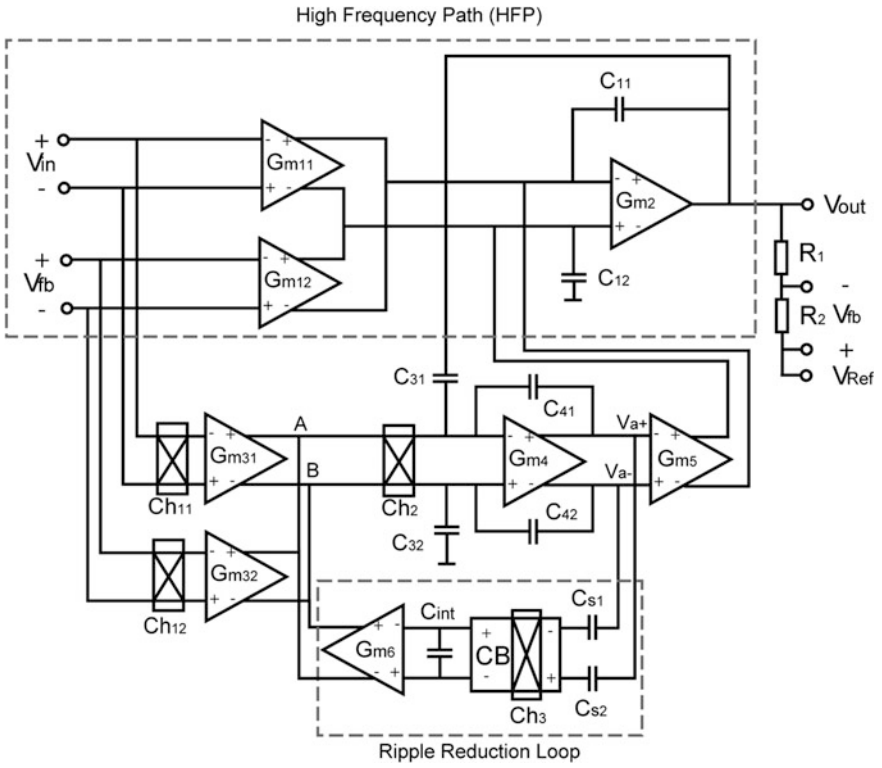

Fig. 7.2 Schematic of a multipath current feedback instrumentation amplifier (CFIA)

DC gain while its own offset is reduced by chopping. Both the chopper stabilization technique and the current feedback topology have been described in Chap. 2. A ripple reduction loop (RRL) is employed to suppress the chopping ripple of the LFP, as also explained in Chap. 2, and thus, a notch is formed [15]. However, this notch is buried by the HFP, so that a smooth transfer function can be obtained [12]. The CFIA achieves state-of-the-art performance in terms of precision. However, its 715 μW power consumption is too high for wireless sensor nodes. The use of four input and feedback transconductances also limits its noise efficiency. To increase this, the HFP can be removed at the cost of decreased bandwidth and a notch in the transfer function, as presented by Wu in [15]. Even so, the optimal noise efficiency will still be limited by the need for two input and feedback transconductances.

To improve gain accuracy, which is limited by the mismatch between G_{m31} and G_{m32} as explained also in Chap. 6 (typically 0.5 %), the transconductor swapping technique [15] and resistive degeneration can be applied. However, the first technique is limited by the CM biasing condition of G_{m31} and G_{m32}, and the second technique results in lower power efficiency.

7.2.2 State-of-the-Art IAs for AC Biomedical Sensing

Many IAs for biomedical sensing can be found in the literature [16–20]. In this section, several of the most recently published designs will be briefly introduced.

7.2.2.1 Capacitively Coupled Instrumentation Amplifiers

A capacitively coupled IA (CIA) was published by Harrison in 2006 [16]. The topology is shown in Fig. 7.3. With the input capacitive coupling, the electrode offset was completely blocked. This was a huge advantage especially for dry electrodes, whose offset can be larger than a few hundreds of millivolts. The high-pass corner of the IA was determined by the input capacitor and the biasing resistor $R_{b1,2}$, which was implemented as a pseudo-resistor [16]. Due to its simplicity, the power efficiency was very high. The drawbacks of the work included a relatively low CMRR which was determined by capacitor mismatch and the unsuppressed $1/f$ noise in the signal bandwidth.

To improve the low-frequency noise of the above design, choppers were added around G_{m1} in [17] by Verma in 2010 (Fig. 7.4). However, the charge injection and clock feed-through of the input chopper switches resulted in an input current with a DC value I_{in}, which is normally in the order of tens of Pico Amp to hundreds of Pico Amp. This input current then flowed through R_{b1}, resulting an output offset voltage. Since R_{b1} are usually very large (tens to hundreds of Giga Ohm), the resulting output offset voltage was not negligible. To overcome this issue, a DC servo loop was employed, as shown in Fig. 7.4. This loop integrated the output offset voltage, converted it into a DC current via R_{b2}, and then fed it back to cancel the input current caused by CH_{in}. Apart from the input current, chopping caused another problem which was due to the shot noise of the CH_{in}. A detailed analysis of this noise by Xu can be found in [18]. When referred to the input, this shot noise (a current noise) was converted into voltage by the input capacitors $C_{in1,2}$. To reduce this voltage noise, the value of $C_{in1,2}$ must be sufficiently large. In this case [17], $C_{in1,2}$ were chosen to be 1nF. These capacitors are too big to be integrated on

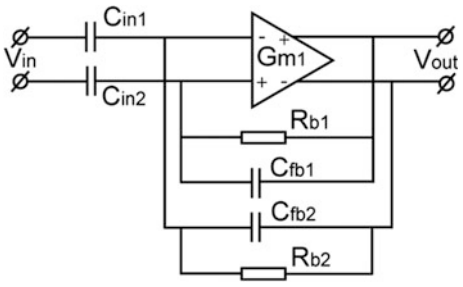

Fig. 7.3 Schematic of the capacitively coupled instrumentation amplifier by Harrison [18]

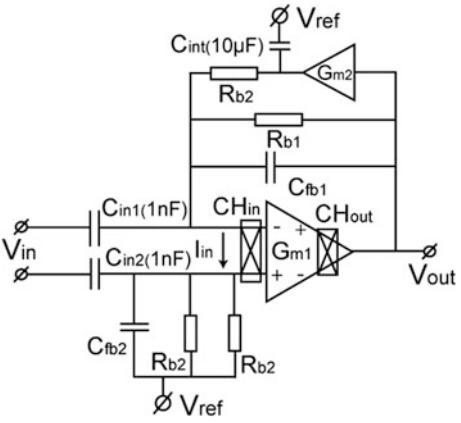

Fig. 7.4 Schematic of the capacitively coupled instrumentation amplifier by Verma [19]

chip. Also they degrade the AC input impedance of the amplifier significantly. For instance, the bandwidth of the biosignals can be 100 Hz; with 1 nF input capacitors, the input impedance at 100 Hz is only 1.7 MΩ.

To further increase the input impedance and also improve the limited CMRR due to the capacitor mismatch, a third paper was published by Xu in 2011 [18]; the schematic is shown in Fig. 7.5. The amplifier employed an impedance boosting technique, the principle of which was based on an impedance boosting loop, which will be presented in the next section. This loop produced a signal current which was ideally equal to the signal current drawn by C_{in}. Thus, the signal source did not need to supply any current, which means the input impedance of the amplifier was ideally infinite. To improve the CMRR, this work employed the back-end CMFB circuit shown in Fig. 7.5. The CM sense block produced an output voltage equal to the input CM voltage of V_{in} and fed it back to the positive terminal of G_{m1} to cancel the AC–CM interference. This amplifier also suffered from the shot noise of CH_{in}, and thus, a relatively large C_{in} (300 pF) was used.

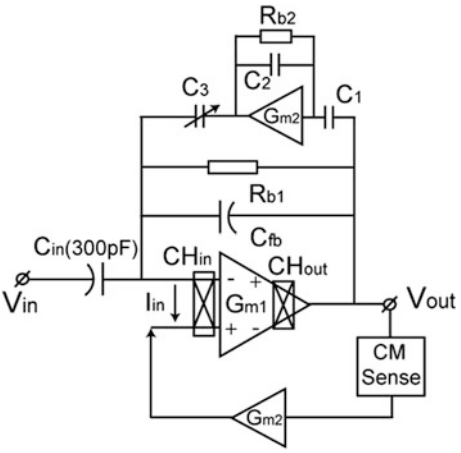

Fig. 7.5 Schematic of the capacitively coupled instrumentation amplifier by Xu [18]

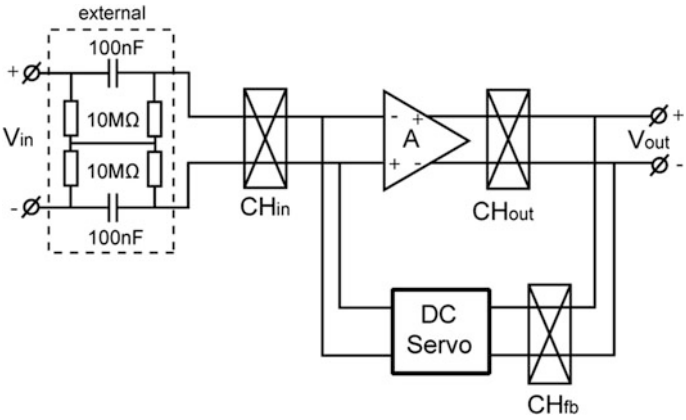

Fig. 7.6 Simplified block diagram of a chopper instrumentation amplifier for biomedical readout

7.2.2.2 Chopper Instrumentation Amplifier

A chopper instrumentation amplifier was published by Yazicioglu in 2011 [19]. A simplified block diagram of this amplifier is shown in Fig. 7.6. It consisted of an external high-pass filter, an IA, and a DC servo loop. To reduce the 1/*f* noise, chopping was employed. The chopping ripple was first demodulated and then sensed by a DC servo loop (DSL) which corrected the offset of the amplifier. This work obtained a high CMRR (100 dB). Due to the input high-pass filter, large electrode offset (>300 mV) was tolerated; thus, it can be used for both dry and wet electrodes. However, the input differential impedance was limited by the high-pass filter. Moreover, the use of large external components is not favorable for highly integrated low-cost wireless sensor nodes.

7.2.2.3 Capacitively Coupled Chopper Instrumentation Amplifier

In 2007, Denison published the first CCIA, as mentioned in Chap. 6 [1]. A simplified block diagram of this CCIA is shown in Fig. 7.7, which consisted of a single-ended CCIA and an output buffer which also served as a second-order low-pass filter. The basic working principle of a CCIA has been explained in Chap. 3. To suppress the electrode offset, a DC servo loop was employed which consisted of a switched-capacitor (SC) integrator and two feedback capacitors ($C_{hp1,2}$). The electrode offset was first amplified by the CCIA, integrated by the SC integrator, and then fed back through $C_{hp1,2}$. The SC integrator continued integrating until the output of the CCIA was DC-free. In this way, a high-pass transfer function was realized. In this work, the maximum acceptable electrode offset was limited to around 50 mV, since an amplified version of this offset would appear at the output of the SC integrator, which had to be lower than the supply. However, this was still sufficient for wet electrodes.

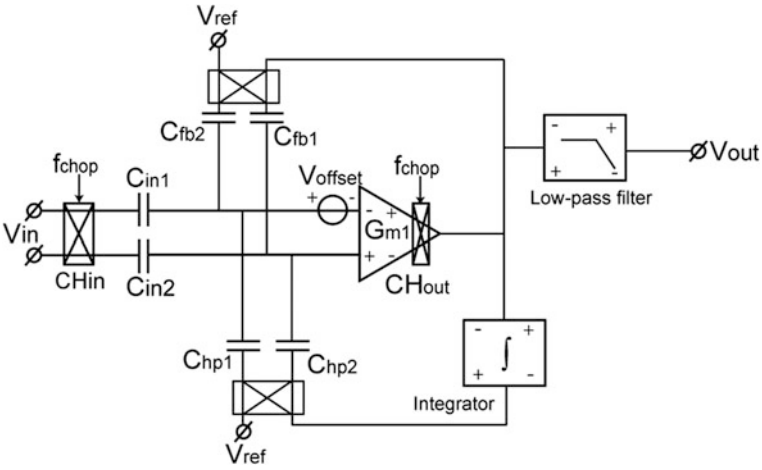

Fig. 7.7 Block diagram of the capacitively coupled instrumentation amplifier by Denison [1]

Due to chopping, the up-modulated offset and 1/*f* noise of G_{m1} resulted in ripple. To suppress this, an output buffer, which was also a low-pass filter, was employed at the output of the CCIA. However, the drawbacks of this have been explained in Chap. 2, which include the need for large passive components and the existence of residual offset. Other drawbacks of this work included relatively low input impedance, which was determined by the SC resistor formed by the input chopper and the capacitor; and a relatively large chip area, which was occupied by the SC integrator (100 pF) and the output buffer (200 pF and 90 MΩ).

7.2.3 Conclusions

From the above introduction, it evident that for DC measurement, the power efficiency, and the gain accuracy of the state-of-the-art IAs can still be improved. For AC biomedical measurement, although input capacitive coupling is very popular since it can completely block the DC electrode offset, the input capacitors are often too big (hundreds of picofarad to tens of nanofarad) especially for wireless sensor nodes. In the following section, a CCIA aimed at coping with both problems will be presented.

7.3 Design of a CCIA for Wireless Sensor Nodes

A block diagram of the basic structure of the proposed CCIA is shown in Fig. 7.8, which is similar to that has been introduced in Chap. 6. It consists of a two-stage Miller-compensated opamp (G_{m1} and G_{m2}), a capacitive bridge ($C_{in1,2}$ and $C_{fb1,2}$),

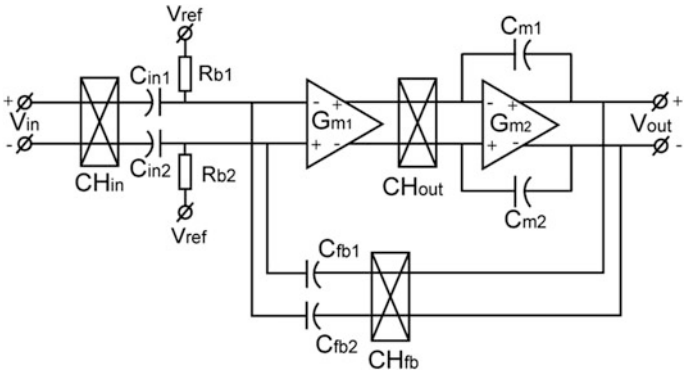

Fig. 7.8 Block diagram of the basic structure of the proposed CCIA

and three choppers (CH_{in}, CH_{out} and CH_{fb}). The basic working principle of a CCIA can be found in Chap. 3. As mentioned in Chap. 1, a disadvantage of the CCIA for both DC and AC measurements is the relatively low input impedance, which is determined by the SC resistance formed by the input chopper and capacitors. To solve this problem, an input impedance boosting loop is proposed which consists of a positive feedback path connected between the input and the output of the CCIA (Sect. 7.3.1). It converts the output voltage into current which is injected back into the signal source. This current partially compensates for the current drawn from the signal source by the SC resistor formed by CH_{in} and $C_{in1,2}$, thus increasing the input impedance of the CCIA.

To suppress the chopping ripple, an RRL is employed. Based on the comparison between the two RRL implementations presented in Chaps. 5 and 6, the switched-capacitor (SC) RRL is preferred for wireless sensor nodes since it is more area-efficient.

To measure biomedical AC signals, a band-pass transfer function is required to reject the electrode offset. Thus, a DC servo loop (DSL) is added which shares the same working principle as that employed in [1]. This loop can be turned off when the CCIA is used in DC mode. However, the DSL presented in [1] consumes a large chip area. In the proposed CCIA, this will be reduced significantly by employing an area-efficient SC integrator (Sect. 7.3.3).

7.3.1 Input Impedance Boosting Loop

A block diagram of the CCIA with the impedance boosting loop, also known as a positive feedback loop (PFL), is shown in Fig. 7.9. The loop comprises a chopper CH_{pf} and two feedback capacitors $C_{pf1,2}$ which provide positive feedback to the input of the CCIA. In the ideal situation, the loop generates a current $I_{pf1,2}$ which is equal to $I_{fb1,2}$, so that no input current is drawn from the signal source and the input

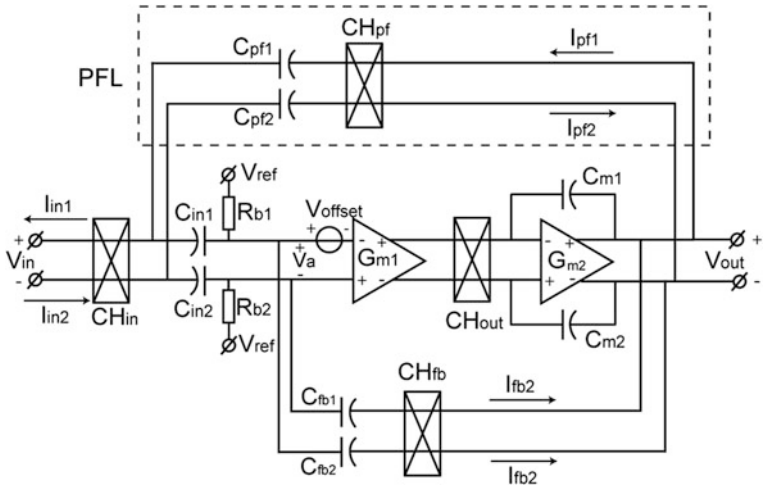

Fig. 7.9 Schematic of the CCIA with the input impedance boost loop

impedance of the CCIA is infinite. The value of $C_{\mathrm{pf1,2}}$ for infinite input impedance can be calculated by making $I_{\mathrm{pf1,2}}$ and $I_{\mathrm{fb1,2}}$ equal:

$$\begin{aligned} I_{\mathrm{pf1,2}} &= 2(V_{\mathrm{out}} - V_{\mathrm{in}}) \times f_{\mathrm{chop}} \times C_{\mathrm{pf1,2}} = 2V_{\mathrm{out}} \times f_{\mathrm{chop}} \times C_{\mathrm{fb1,2}} = I_{\mathrm{fb1,2}} \\ &\Rightarrow C_{\mathrm{pf1,2}} = \frac{C_{\mathrm{in1,2}}}{G-1}. \end{aligned} \tag{7.1}$$

The loop loads the CCIA, since the current flowing through it has to be supplied by the CCIA. The equivalent loading resistance is around $\frac{1}{2f_{\mathrm{chop}} \times C_{\mathrm{pf1,2}}}$. This loading is equal to that of the negative feedback path ($C_{\mathrm{fb1,2}}$).

7.3.2 SC Ripple Reduction Loop (SC RRL)

A schematic of the SC RRL is shown in Fig. 7.10 with a timing diagram. Since the working principle of the SC RRL has already been explained in detail in Chap. 5, only a brief explanation will be given here. The loop consists of an SC integrator, a compensation transconductance (G_{m4}), and an integrator built around G_{m2}. The SC integrator comprises sensing capacitors $C_{\mathrm{s1,2}}$, a demodulation chopper $\mathrm{CH_{RRL}}$, integration capacitors $C_{\mathrm{int1,2}}$, auto-zero capacitors $C_{\mathrm{az1,2}}$, and a single-stage opamp G_{m3}. The switching clock frequency f_{s} is chosen to be half of f_{chop}. Thus, during Φ_1, a full cycle ripple can be detected by the RRL. $C_{\mathrm{s1,2}}$ converts the ripple voltage into an AC current which is then demodulated by $\mathrm{CH_{RRL}}$ and integrated on $C_{\mathrm{int1,2}}$. The voltage on $C_{\mathrm{int1,2}}$ is then converted into a current by G_{m4} to compensate for the offset current of G_{m1}. During Φ_2, $C_{\mathrm{s1,2}}$ is shorted to ground so that no ripple current

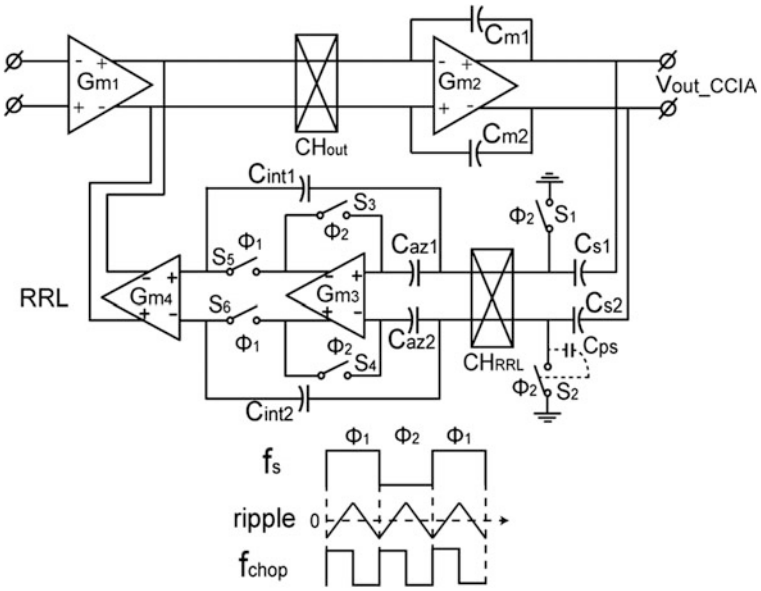

Fig. 7.10 Schematic of the switch-capacitor RRL and its timing diagram

is integrated. G_{m3} is configured in a unity-gain configuration so that its offset is sampled and stored on $C_{az1,2}$. During this time, $C_{int1,2}$ is first disconnected from the output of G_{m3}—holding the voltage set at the end of the final Φ_1, and then connected to the input of G_{m4}.

In this way, the correct compensating current is steadily injected into G_{m1} during both phases. In the ideal case, the compensating current fully compensates for the offset current of G_{m1}, leaving no output ripple at the steady state.

As explained in Chaps. 2 and 5, the noise of the RRL can be designed negligible by choosing a much smaller G_{m4} than G_{m1}. The *kT/C* noise associated with the auto-zeroing of G_{m3} is also negligible since it will be eventually up-modulated and filtered by the integrator built around G_{m3}.

7.3.3 DC Servo Loop (DSL)

As mentioned above, in biomedical applications, an electrode offset that is much larger than the AC signals is present and should be suppressed by the CCIA. Although a high-pass transfer function can be easily obtained by disabling the choppers around the CCIA, the degraded CMRR due to capacitor mismatch is undesirable, as in [18]. To obtain a high CMRR, chopping is maintained, and a high-pass transfer function is realized by implementing a DSL, as in [1]. The low-pass characteristic is automatically conferred by the limited bandwidth of the

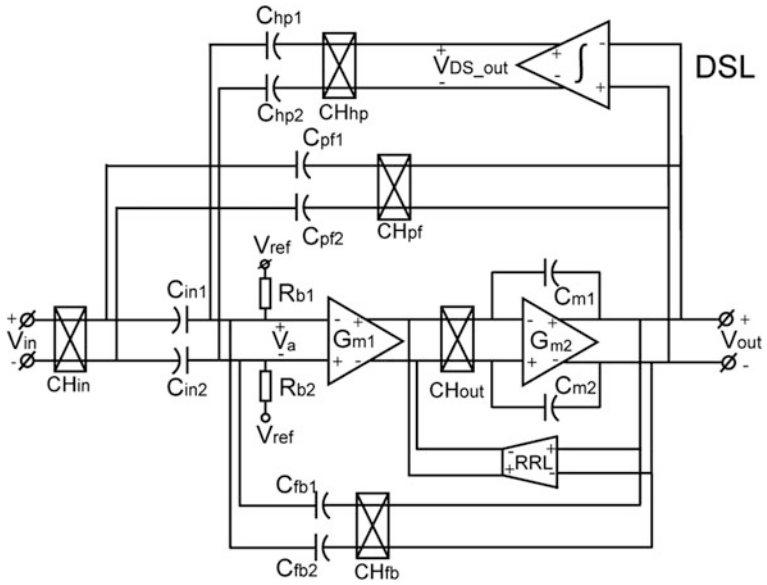

Fig. 7.11 Schematic of the CCIA with the DC servo loop (DSL)

CCIA, which should be larger than the maximum ECG/EEG signal bandwidth (around 100 Hz). A block diagram of the CCIA with this DSL is shown in Fig. 7.11. The DSL comprises an integrator which amplifies the DC signal at the output of the CCIA; a chopper CH_{hp} which up-modulates the amplified DC signal; and capacitors $C_{hp1,2}$ which feed the up-modulated signal to the CCIA virtual ground. The integrator will continue integrating until the signal at the output of the CCIA is DC-free. The DSL creates a high-pass corner f_{hp} which is given by [1]:

$$f_{hp} = \frac{C_{hp1,2}}{C_{fb1,2}} \times f_{0DSL}, \tag{7.2}$$

where f_{0DSL} is the unity-gain frequency of the integrator in the DSL. In ECG and EEG applications, f_{hp} is usually required to be around 0.5 Hz. If $C_{hp1,2}/C_{fb1,2}$ is unity, f_{0DSL} must then be equal to 0.5 Hz. This usually requires large capacitors and/or resistors which can occupy a large chip area and are thus not suitable for wireless sensor nodes. For instance, if a first-order RC integrator is employed, an input resistor of 10 MΩ will require an integration capacitor of 33 nF. Moreover, due to process variation, the unity-gain frequency of this integrator will not be accurate without trimming. An SC integrator is more accurate, but still requires the use of large capacitors. If the conventional SC integrator shown in Fig. 7.12 is employed, its unity-gain frequency f_0 can be estimated by [21]:

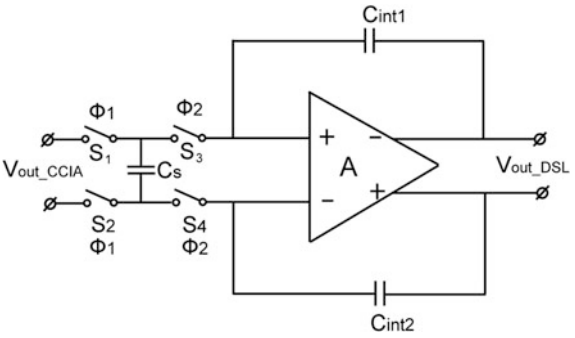

Fig. 7.12 Block diagram of a standard switched-capacitor integrator

$$f_0 = \frac{f_{\text{swi}} \times C_{\text{s1,2}}}{2\pi \times C_{\text{int1,2}}}, \tag{7.3}$$

where f_{swi} is the switching frequency for switches S_1–S_4. Thus, if f_{swi} = 2.5 kHz and $C_{\text{s1,2}}$ = 100 fF, $C_{\text{int1,2}}$ must be 83 pF. This means the total capacitance of the fully differential implementation of such an integrator is 166 pF. However, the above estimation has been made is under the assumption that $C_{\text{hp1,2}}/C_{\text{fb1,2}}$ is unity, which may not be valid in actual design situations. The reasons are that the DSL amplifies the input electrode offset, which will appear at the output of the DSL ($V_{\text{out\_DSL}}$) and can be expressed by:

$$V_{\text{eomax}} = \frac{C_{\text{hp1,2}}}{C_{\text{in1,2}}} \times V_{\text{out\_DSL}}, \tag{7.4}$$

where V_{eomax} is the maximum accepted electrode offset (typically 50 mV for wet electrodes), and $V_{\text{out\_DSL}}$ is maximally equal to the supply voltage (1 V in this design). Thus, in this design, $C_{\text{hp1,2}}/C_{\text{in1,2}}$ should be 1/20. According to the specification shown in Table 7.1, the CCIA should provide a gain of 100, which is determined by $C_{\text{in1,2}}/C_{\text{fb1,2}}$. As a result, $C_{\text{hp1,2}}/C_{\text{fb1,2}}$ must be equal to 5. Consequently, according to Eq. (7.2), the unity-gain frequency of the integrator in the DSL must be 0.1 Hz. To meet this challenge, a very large time constant (VLT) SC integrator [22] is employed in this work with minimum chip area. Its working principle is introduced in the following section.

7.3.3.1 A very large time constant SC integrator (VLT SC integrator)

The VLT SC integrator was first published by Nagaraj in [22]. Its block diagram is shown in Fig. 7.13. The integrator comprises an opamp and a surrounding capacitor network ($C_{\text{a1,2}}$, $C_{\text{A1,2}}$, $C_{\text{a1,2'}}$, and S_1–S_7). All switches in the capacitor network are driven at a switching frequency f_{sVLT}. The integrator is operated as follows. First, an integration cycle is divided into two phases: Φ_1 and Φ_2. In the time domain, Φ_1 is

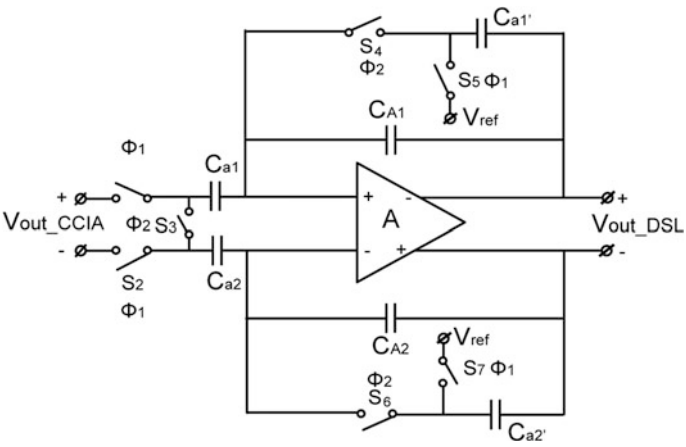

Fig. 7.13 Schematic of the very large time constant integrator

defined from (n) to (n + 1/2) where n the number of clock cycles; while Φ_2 is defined from (n + 1/2) to (n + 1). In Φ_1, the input signal is first sampled on $C_{a1,2}$. At the end of Φ_1, a charge equal to $V_{in}(n + 1/2)\ C_{a1,2}$ is pushed into $C_{a1,2}$, where $V_{in}(n + 1/2)$ is the signal at the end of Φ_1. As a consequence, the charge on $C_{A1,2}$ changes accordingly, resulting in an output voltage step $\Delta V_{out}(n + 1/2)$ given by [23]:

$$\Phi_1 : \Delta V_{\text{out}}(n+\frac{1}{2}) = -\frac{V_{\text{in}}(n+\frac{1}{2}) \times C_{\text{a1,2}}}{C_{\text{A1,2}}}. \tag{7.5}$$

Meanwhile, $C_{a1,2}'$ samples this output voltage, acquiring a charge equal to $\Delta V_{out}(n + 1/2)\ C_{a1,2}'$. In Φ_2' $C_{a1,2}$ is discharged. The charge pushed into $C_{a1,2}$ in Φ_1 is now completely pulled out, leaving an output voltage step equal to exactly $-\Delta V_{out}(n + 1/2)$, thus canceling the voltage step obtained in Φ_1. However, a tiny difference is made by $C_{a1,2}'$, which is now connected as a feedback capacitor in parallel with $C_{A1,2}$. Thus, the charge stored on $C_{a1,2}'$ in Φ_1 must now be redistributed between $C_{a1,2}'$ and $C_{A1,2}$. This results in a small output voltage step calculated by:

$$\Phi_2 : \Delta V_{\text{out}}(n+1) = \frac{\Delta V_{\text{out}}(n+1/2) C_{\text{a1,2}'}}{C_{\text{A1,2}} + C_{\text{a1,2}'}}, \tag{7.6}$$

Where $\Delta V_{out}(n + 1)$ is the total output voltage change after one clock cycle. Substituting Eq. (7.5) into Eq. (7.6), $\Delta V_{out}(n + 1)$ can be calculated by:

$$\Delta V_{\text{out}}(n+1) = -\frac{V_{\text{in}}(n+\frac{1}{2}) C_{\text{a1,2}} C_{\text{a1,2}'}}{C_{\text{A1,2}}(C_{\text{A1,2}} + C_{\text{a1,2}'})}, \tag{7.7}$$

Usually, $C_{a1,2}'$ is equal to $C_{a1,2}$ and is chosen to be much smaller than $C_{A1,2;}$ thus, the integrator only integrates a fraction of the input signal per clock cycle. As a result, the time constant of the integrator is greatly increased. Its unity-gain frequency f_{0VLT} is obtained by calculating its transfer function in the z domain, where $(n + x)$ can be substituted by z^{-x} and $C_{a1,2} = C_{a1,2}'$ [23]:

$$H(z) \approx -\left(\frac{C_{a1,2}}{C_{A1,2}}\right)^2 \frac{Z^{-1/2}}{1 - Z^{-1}}. \tag{7.8}$$

By making H(z) equal to unity, f_{0VLT} can be computed as [23]:

$$f_{0VLT} = \frac{f_{sVLT} C_{a1,2}^2}{2\pi C_{A1,2}^2}, \tag{7.9}$$

where f_{sVLT} is the switching frequency of the VLT integrator. This offers a significant advantage over a normal SC integrator. To achieve the 0.1 Hz unity-gain frequency, with a switching frequency f_{sVLT} = 2.5 kHz, and $C_{a1,2} = C_{s1,2}$ = 100 fF, a standard integrator requires a $C_{int1,2}$ of 415 pF according to Eq. (7.3), while a VLT integrator only needs 2.8 pF ($C_{A1,2}$) according to Eq. (7.9).However, this area efficiency comes at a price. When taking the offset of the integrator opamp V_{off} into account, the output of the VLT integrator is calculated by Nagaraj [23]:

$$V_{out\_DSL}(z) = -\left(\frac{C_{a1,2}}{C_{A1,2}}\right)^2 \left(V_{out}(z) + V_{off}\frac{C_{A1,2}}{C_{a1,2}}\right) \frac{Z^{-1/2}}{1 - Z^{-1}}. \tag{7.10}$$

According to this, the offset of the integrator opamp is amplified by $C_{A1,2}/C_{a1,2}$, which is generally much larger than one. The same factor is expected for low-frequency 1/*f* noise as well. Also, charge injection and clock feed-through errors would result in residual offset, so this offset is again amplified. Thus, the VLT integrator is rather inaccurate and is sensitive to all sorts of errors. A fully differential structure is recommended to limit the charge injection and clock feed-through errors. A symmetrical layout of all the switches is also necessary (see Appendix A). To suppress the amplified offset and 1/*f* noise of the integrator opamp, chopping is employed, which is shown in Fig. 7.14. CH_{DS1} and CH_{DS2} are synchronized with all the other choppers in the CCIA. A timing diagram is also shown in Fig. 7.14. f_{sVLT} is chosen to be $2f_{chop}$, and the sampling point is at the zero-crossing point of any residual ripple that can be expected at the output of the CCIA (Fig. 7.14). The up-modulated offset and 1/*f* noise of G_{m5} again result in ripple. Thus, another RRL is employed which is identical to that introduced in Sect. 7.3.2. The complete CCIA is shown in Fig. 7.15.

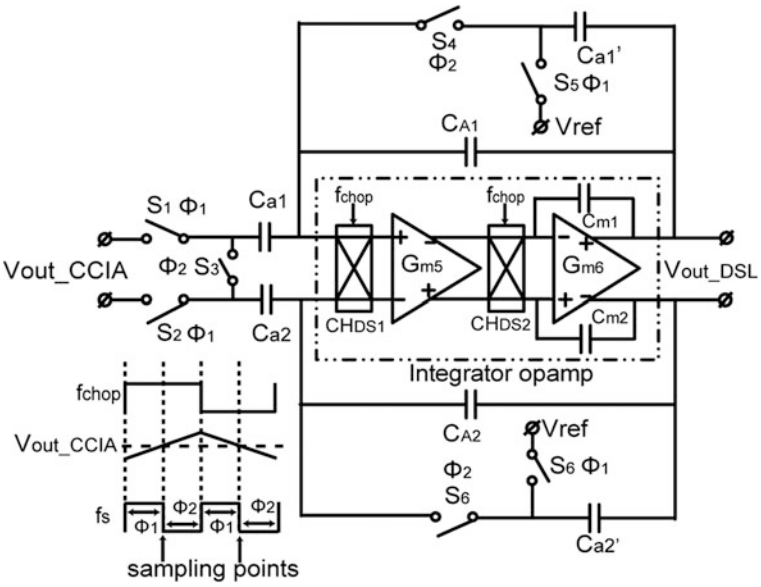

Fig. 7.14 Schematic of the chopper VLT SC integrator

7.4 Realization

This section gives implementation details to achieve the specifications listed in Table 7.1. First, the global parameters such as the chopping frequency f_{chop} and the capacitive bridge are presented. Also, in 65 nm CMOS technologies, two types of transistors are available. Thus, choosing the appropriate type is of critical importance. Later, the implementation details of the CCIA's opamp, the biasing resistors $R_{b1,2}$, the PFL, the RRL, and the DSL will be given.

7.4.1 Global Parameters (Chopping Frequency, Capacitive Bridge, and Transistor Type)

As explained in Chap. 6, several considerations should be taken into account when choosing f_{chop}: it should be far away from the signal band; it should not be too high as it could result in excessive residual offset due to charge injection and clock feed-through errors; and it should not be too low as it could lead to insufficient filtering of the residual ripple due to the circuit non-ideality in the RRL. In this design, f_{chop} for DC mode is chosen to be 5 kHz. This is sufficiently far away from the 100 Hz signal band. However, this is much lower than that in the previous design. The main consideration is that due to the ultra-low bias current of the CCIA,

the whole CCIA is much slower than the one presented in Chap. 4, especially G_{m1}, which is between the input and output choppers. As a consequence, f_{chop} should also be low to ensure sufficient gain of G_{m1} at f_{chop}. In AC mode, f_{chop} is further reduced to 1.25 kHz. This mainly lowers the switching frequency of the DSL integrator, which should be $2\times f_{chop}$, as explained in Sect. 7.3. A slow switching frequency eases the design of the DSL integrator according to Eq. (7.9).

The capacitors used to implement the feedback network are metal–metal capacitors. For matching purposes ($0.1 \sim 0.2$ %), $C_{in1,2}$ is chosen to be 12 pF, and $C_{fb1,2}$ is 120 fF for a fixed gain of 100, as required for the application (Table 7.1). Exactly as in the CCIA presented in Chap. 4, the bottom plates of $C_{in1,2}$ and $C_{fb1,2}$ should be connected to the input and output, respectively, rather than the virtual ground of the CCIA. Otherwise, the heavy parasitic capacitances at the bottom plates will increase the noise of the CCIA according to Eq. (3.10).

The whole CCIA was implemented in a standard 65 nm CMOS technology with a supply voltage of 1 V. There are two types of transistors in the 65 nm CMOS process: the thin-oxide transistors and the thick-oxide transistors. Although some benefit is gained from their low threshold voltages and small minimum feature size, the thin-oxide transistors suffer from gate leakage current and low intrinsic gain, which limit their use in precision analog designs. For instance, due to noise considerations, the resistance of the bias resistors $R_{b1,2}$ is calculated to be around 10 GΩ (Fig. 7.15). Thus, a 100 pA gate leakage from the input transistors of G_{m1} is enough to cause its input CM voltage to clip. Even if this current can be reduced by decreasing the area of the input transistors, for instance, the mismatched gate leakage current can still cause offset. Moreover, when used to implement the

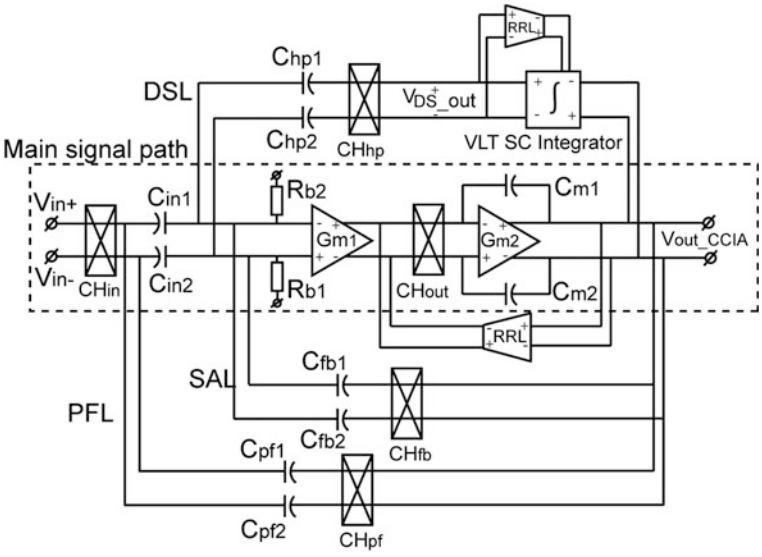

Fig. 7.15 Schematic of the complete CCIA

switches in the VLT integrator, the leakage current will result in voltage drift (especially with a low switching frequency) and residual offset (in a similar manner as mismatched charge injection and clock feed-through). These could cause serious problems and degrade the accuracy of the circuit. Lastly, the low intrinsic gain rules out the use of the thin-oxide transistors, since the effectiveness of several structures (such as the RRL and the DSL) rely on a high open-loop gain. In the end, the thick-oxide transistors were employed throughout the CCIA despite their relatively high threshold voltage ($\sim$0.6 V).

7.4.2 Opamp of the CCIA

The opamp of the CCIA is a simple two-stage Miller-compensated amplifier (G_{m1}, G_{m2} and C_m). Its schematic is shown in Fig. 7.16.

The DC gain of the CCIA opamp must be large enough not to cause any significant gain error. This can be estimated by:

$$G = \frac{A_0}{1 + A_0 C_{fb1,2}/C_{in1,2}}, \tag{7.11}$$

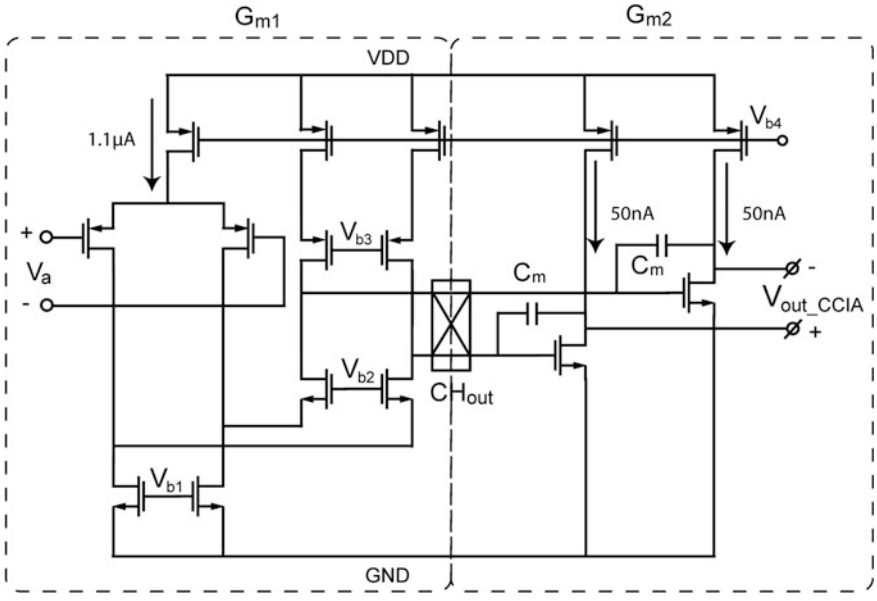

Fig. 7.16 Schematic of the CCIA opamp

where A_0 is the DC open-loop gain of the CCIA, and G is the closed-loop gain of the CCIA. The simulated DC gain of the two-stage Miller-compensated CCIA opamp is around 100 dB, which according to Eq. (7.11) corresponds to an absolute gain error of <0.1 % for G = 100. Meanwhile, the layout parasitic, process spread, and variation of $C_{in1,2}/C_{fb1,2}$ also determines the gain accuracy, which is expected to be around 0.1 %. The noise of the CCIA is dominated by the noise of the input stage of G_{m1}. The input PMOS differential pair is biased in weak inversion. It consumes 1.1 μA, 61 % of the total supply current, and, consequently, a 55 nV/$\sqrt{\text{Hz}}$ simulated noise voltage density V_{nopamp} of the input stage is obtained. Thus, the CCIA's rms noise within the signal band (100 Hz) is 0.55 μV, which should be less significant compared to the expected residual offset (a few microvolts). The bias currents of other stages are shown in Fig. 7.16. With $C_{in1,2}/C_{fb1,2}$ = 100 and neglecting parasitic effects, the input-referred noise of the CCIA is essentially equal to V_{nopamp}, according to Eq. (3.7). The Miller capacitors C_m are chosen to be 30 pF, with G_{m1} = 13 μS, and the unity-gain frequency of the CCIA is about 70 kHz.

7.4.3 Biasing Resistor R_b

The biasing resistor $R_{b1,2}$ shown in Fig. 7.15 is required to fix the input CM DC level of G_{m1} As indicated in Chaps. 5 and 6, NMOS transistors biased in the subthreshold region can be used as area-efficient and transient-free biasing resistors. Although they are nonlinear during large CM transients, they are suitable for low-frequency small-signal sensor readout, where the CM level of the signal is mostly constant. As mentioned at the beginning of Sect. 7.4, the chopping frequency in AC and DC modes is different. With f_{chop} = 1.25 kHz in AC mode, $R_{b1,2}$ must be approximately 10 GΩ to obtain an input noise contribution of about 14 nV/$\sqrt{\text{Hz}}$, according to Eq. (3.3), which is negligible compared to that of the whole CCIA (∼55 nV/$\sqrt{\text{Hz}}$). This becomes even more negligible (3.5 nV/$\sqrt{\text{Hz}}$) with f_{chop} = 2.5 kHz in DC mode.

7.4.4 Impedance Boosting Loop or Positive Feedback Loop (PFL)

With the CCIA configured with a fixed gain of 100, $C_{in1,2}$ = 12 pF and $C_{fb1,2}$ = 120 fF, $C_{pf1,2}$ has to be 121.21 fF to reach an infinite input impedance, according to Eq. (7.1). Since this is difficult to layout exactly, in this work, $C_{pf1,2}$ is chosen to be equal to $C_{fb1,2}$. The compromised boosted input impedance of the CCIA is then given by:

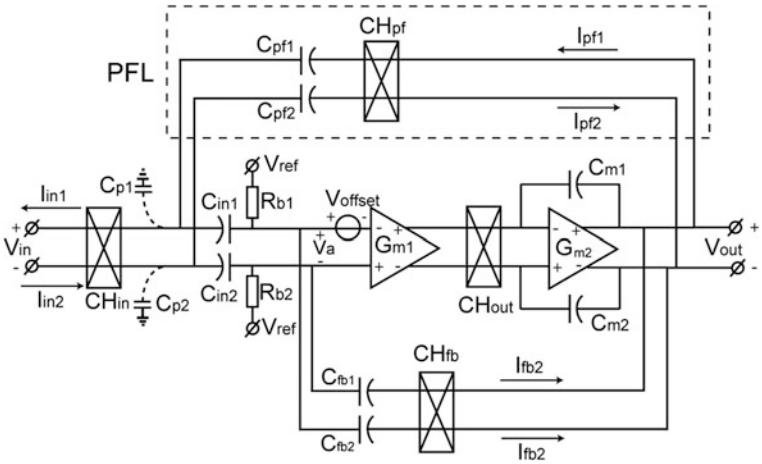

Fig. 7.17 Schematic of the capacitively coupled instrumentation amplifier with the positive feedback loop (PFL)

$$Z_{\text{in\_pf}} = \frac{V_{\text{in}}}{I_{\text{in\_pf}}} = \frac{G}{2f_{\text{chop}} \times C_{\text{in1,2}}} = 100Z_{\text{in}}, \tag{7.12}$$

where Z_{in} is the original input impedance, $Z_{\text{in\_pf}}$ is the boosted input impedance, and $I_{\text{in\_pf}}$ is the net current drawn from the signal source. However, in practice, the parasitic capacitance $C_{\text{p1,2}}$ located between the bottom plate and ground of $C_{\text{in1,2}}$ shown in Fig. 7.17 will further limit the input impedance. CH_{in} and $C_{\text{p1,2}}$ act as an equivalent parasitic resistor with a resistance of $\frac{1}{2f_{\text{chop}} \times C_{\text{p1,2}}}$. The current drawn by this resistor will not be compensated by a PFL dimensioned according to Eq. (7.1). As a result, this parasitic resistor limits the maximum input impedance. In a standard CMOS process, $C_{\text{p1,2}}$ varies between 10 to 40 % of $C_{\text{in1,2}}$. This means that a PFL dimensioned according to Eq. (7.1) will only boost the input impedance by a factor between 2.5× to 10×. To overcome this, the PFL can be designed also to compensate for the extra current flowing through the parasitic resistor. As a result, Eq. (7.1) can be modified as follows:

$$\begin{aligned} I_{\text{pf\_modi1,2}} &= 2(V_{\text{out}} - V_{\text{in}}) \cdot f_{\text{chop}} \cdot C_{\text{pf\_modi1,2}} \\ &= I_{\text{fb1,2}} + 2V_{\text{in}} \cdot f_{\text{chop}} \cdot C_{\text{p1,2}} \\ &= I_{\text{fb1,2}} + I_{\text{p1,2}} \\ &\Rightarrow C_{\text{pf\_modi1,2}} = \frac{C_{\text{in1,2}} + C_{\text{p1,2}}}{G - 1}, \end{aligned} \tag{7.13}$$

where $I_{\text{pf\_modi1,2}}$ is the modified compensating current provided by the PFL, and $C_{\text{pf\_modi1,2}}$ is the optimal value for $C_{\text{pf1,2}}$. In practice, however, the exact value of $C_{\text{p1,2}}$ will be uncertain, and so $C_{\text{pf1,2}}$ can be made adjustable in order to obtain

maximum input impedance. With trimmable $C_{pf1,2}$, an effective boost factor of 10× was achieved [20].

7.4.5 SC RRL

The block diagram of the RRL is shown in Fig. 7.19. As explained in Chap2, the RRL creates a notch in the transfer function of the CCIA. The values of $C_{s1,2}$, $C_{int1,2}$, and the transconductance of G_{m4} determine the width of the notch, which is calculated by [23]:

$$f_{0RRL} = \frac{G_{m4}C_{s1,2}}{2\pi C_{mC_{int1,2}}}. \tag{7.14}$$

With G_{m4} = 0.65 μS, $C_{s1,2}$ = 240 fF, $C_{int1,2}$ = 2.5 pF, and $C_{m1,2}$ = 30 pF, f_{0RRL} is calculated to be around 330 Hz. With either a 5 kHz chopping frequency in DC mode or 1.25 kHz in AC mode, the notch introduced by the RRL is well outside the signal bandwidth. To make the noise of the RRL negligible compared to that of G_{m1}, G_{m4} (Fig. 7.10) is designed to be 0.65 μS, which is 20× smaller than G_{m1}. $C_{az1,2}$ is chosen to be 1.4 pF with the considerations of suppressing charge injection errors from switch $S_{3,4}$ and saving chip area.

G_{m3} employs a telescopic topology to obtain enough DC open-loop gain; its schematic is shown in Fig. 7.18. The ripple suppression factor F of the RRL is [Chap. 5, Eq. (5.6)]:

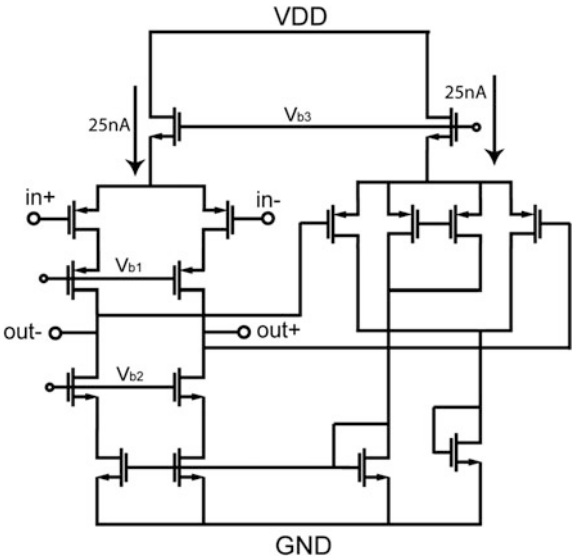

Fig. 7.18 Schematic of the ripple reduction loop switched-capacitor integrator opamp (G_{m3} in Fig. 7.10)

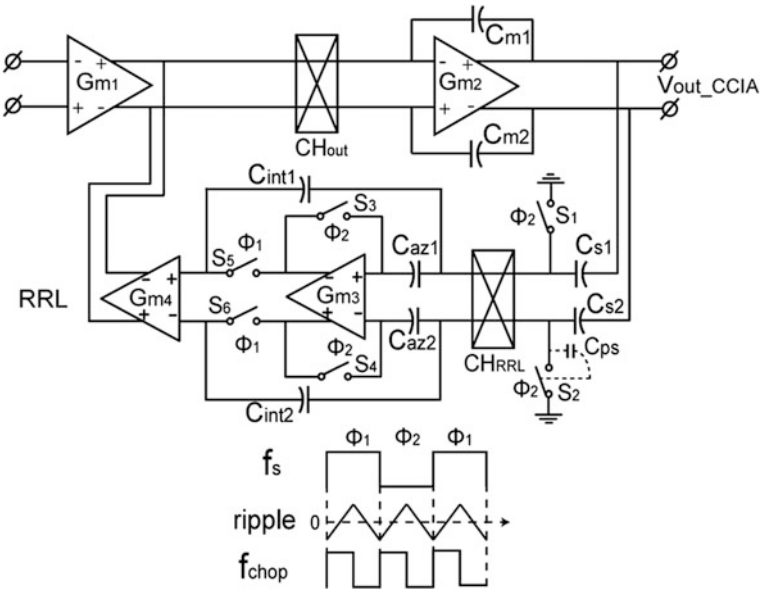

Fig. 7.19 RRL with a parasitic capacitor C_{ps}

$$F = \frac{A_{Gm3} \times G_{m4}}{2C_{m1,2} \times f_{chop}}, \tag{7.15}$$

where A_{Gm3} is the open-loop gain of G_{m3} (Fig. 7.10). The open-loop gain of the G_{m3} is simulated to be around 76 dB. Moreover, with f_{chop} = 5 kHz in DC mode and f_{chop} = 1.25 kHz in AC mode, F is 82 and 94 dB, respectively. To determine whether this suppression factor is sufficient, the unsuppressed ripple should be calculated assuming the offset of G_{m1} is 5 mV:

$$\text{DC mode}: V_{ripple} = \frac{V_{offset} \cdot G_{m1}}{2f_{chop} \cdot C_{m1,2}} = \frac{5\,\text{mV} \cdot 13\,\mu\text{S}}{2 \cdot (5\,\text{kHz}) \cdot 30\,\text{pF}} = 216\,\text{mV}. \tag{7.16}$$

$$\text{AC mode}: V_{ripple} = \frac{V_{offset} \cdot G_{m1}}{2f_{chop} \cdot C_{m1,2}} = \frac{5\,\text{mV} \cdot 13\,\mu\text{S}}{2 \cdot (1.25\,\text{kHz}) \cdot 30\,\text{pF}} = 864\,\text{mV}. \tag{7.17}$$

As a result, with F equal to 82 and 94 dB in DC and AC mode, respectively, the residual ripple should then be within 17 μV in both modes, which is sufficient for the applications.

As explained in Chap. 5, although the offset of the integrator is auto-zeroed, several parasitic error sources remain. First, a voltage spike at the switching frequency at the input of G_{m4} results from the switching between the offset voltage of

G_{m3} and the correct compensation voltage. This spike will eventually turn into a residual ripple at the output of the CCIA. To reduce this effect, the output voltage swing of G_{m3} is limited within only 100 mV by choosing G_{m4}/G_{m1} to equal 1/20, assuming that a maximum G_{m1} offset equals 5 mV. Second, to minimize the charge injection and clock feed-through errors of S_1–S_6, a careful, symmetrical layout is required.

In total, the SC RRL consumes a total capacitance of only 8.5 pF and only 100 nA of current, which is negligible compared to the total current consumption of the CCIA (1.8 µA).

7.4.6 DC Servo Loop (DSL)

A block diagram of the DSL is shown in Fig. 7.15. As explained above, the DSL forms the high-pass transfer function, which is used to null the electrode offset for biomedical sensor readout. According to Eq. (7.4), with V_{eomax} = 50 mV, C_{in} = 12 pF, and V_{DD} = 1 V, C_{hp} must be 600 fF. The rest of the design will thus focus on the VLT integrator.

Very large time constant (VLT) integrator A block diagram of the VLT integrator is shown in Fig. 7.14. According to Eq. (7.5), to achieve a 0.5 Hz high-pass corner, with G = 100, V_{eomax} = 50 mV, and V_{DD} = 1 V, the unity-gain frequency of the VLT integrator should be 0.1 Hz. Since the VLT integrator is sensitive to errors, the sampling capacitor $C_{a1,2}$ (Fig. 7.14) is chosen to be relatively large (240 fF) to reduce the error voltage due to the mismatched charge injection and clock feed-through errors of the switches. With f_{chop} = 1.25 kHz in AC mode, f_{sVLT} should be 2.5 kHz, as explained in Sect. 7.2. Thus, according to Eq. (7.7), the integration capacitor $C_{A1,2}$ must be 15 pF. All the capacitors used in the VLT integrator are metal–metal capacitors.

To ensure that the output of the VLT integrator can swing rail-to-rail, as assumed in Eq. (7.5), the VLT integrator opamp employs a two-stage amplifier with a class-A output stage, as shown in Fig. 7.20. A common-mode feedback (CMFB) circuit regulates the output CM level, which is equal to 0.5 V (half V_{DD}). Due to the ultra-low bias current at the output stage (50 nA), the output impedance is high (hundreds of Mega ohm), and the CM output voltage therefore cannot be sensed by an on-chip resistor as is usually the case [24]. Thus, an SC CMFB is employed [24].

Chopping up-modulates the offset and 1/*f* noise of the integrator's first stage. However, it also brings with it a huge drawback in terms of noise. The shot noise of the chopper switches results in a current noise [20]. When referred to the input of the integrator, this current noise is converted into a voltage by the input sampling capacitors. As the impedance of the capacitors is frequency dependent, this noise voltage is also frequency dependent and becomes more dominant at low frequencies. This will be shown and discussed in the measurement results.

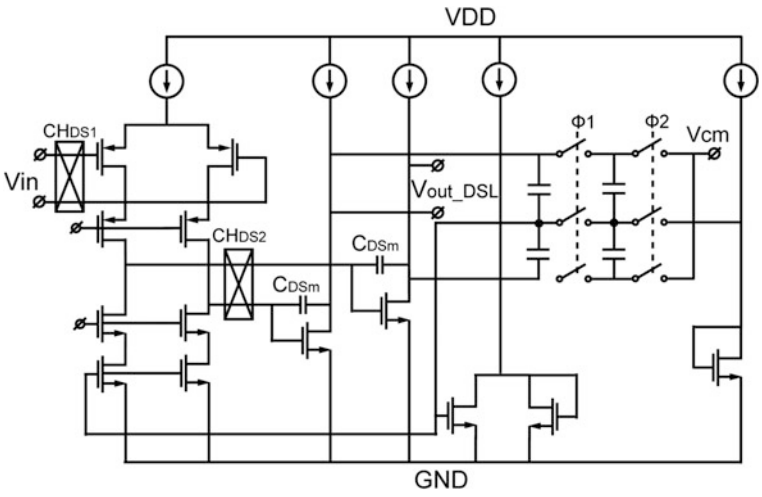

Fig. 7.20 Schematic of the DC servo loop (DSL) integrator with a switched-capacitor CM regulation circuit

7.5 Experimental Results

The circuit was implemented in a 65 nm CMOS technology. The CCIA operated from a 1 V supply from which it drew 1.8 μA without the DSL and 2.1 μA with the DSL. The active chip area was 0.1 mm^2 without the DSL and 0.2 mm^2 with the DSL. A photograph of this is shown in Fig. 7.21, which includes the DSL. With the DSL off, the measured DC CMRR was greater than 134 dB, while the DC PSRR was greater than 120 dB for 20 samples. The worst-case measured offset was 1 μV. A histogram of the offset is shown in Fig. 7.22. The relative DC gain accuracy of the CCIA was better than 0.16 %. A histogram of the gain variation is shown in Fig. 7.23. As shown in Fig. 7.24, the measured output noise spectrum density was 6 μV/$\sqrt{\text{Hz}}$, which is equivalent to an input-referred noise of 60 nV/$\sqrt{\text{Hz}}$. This confirms that the noise was mostly determined by the input stage. Furthermore, the noise floor was flat until 100 MHz, which proves that the 1/*f* noise was effectively removed by chopping. The noise efficiency factor (NEF [18]) was 3.6. After activating the PFL, the measured input impedance increased from 6 to 30 MΩ. The boost factor was only 5 instead of the 100 calculated by Eq. (7.10), due to the presence of parasitic input capacitors, which were not compensated. As has been explained in Sect. 7.4.3, this can be improved by trimming C_{pf} (Fig. 7.17), as in [26]. The RRL reduced the amplitude of the input-referred ripple to less than 3 μV at all the harmonics, which is comparable to the residual offset. This residual ripple, however, is larger than what was presented in Chap. 5. This is mainly due to the layout, which was not as optimized as the layout used in Chap. 5. The transient response of the CCIA to a 500 mV output step is shown in Fig. 7.25. The spikes due to the various switching events are also shown. It can be seen that the output

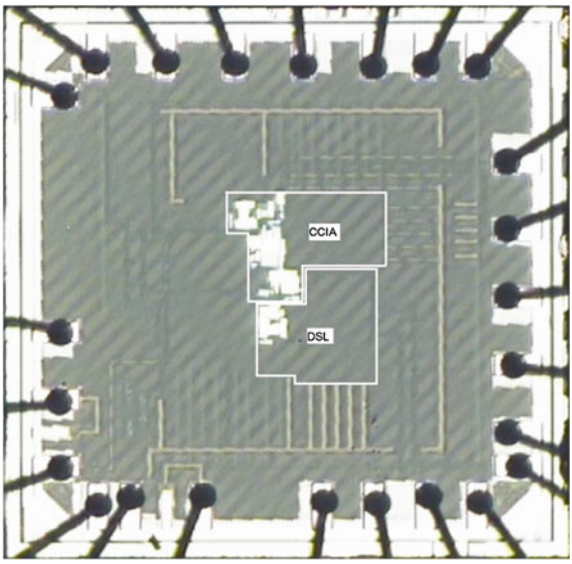

Fig. 7.21 Chip microphotograph

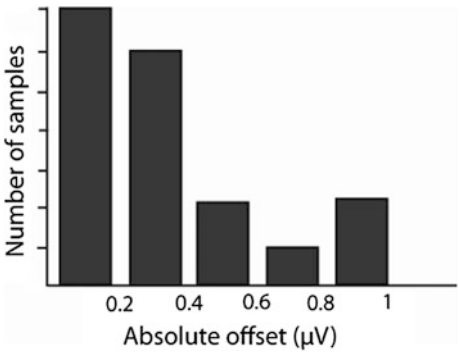

Fig. 7.22 Histogram of the residual offset

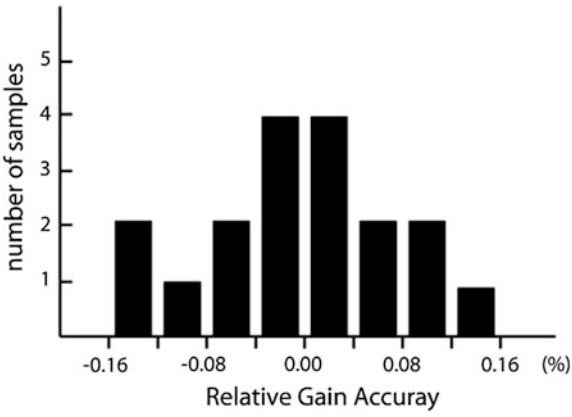

Fig. 7.23 Histogram of the relative gain accuracy

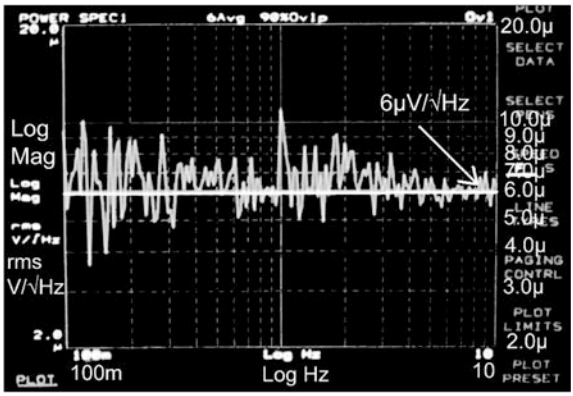

Fig. 7.24 Output noise spectrum of the CCIA in DC mode with a gain of 100 (*Y axis* log format; 2 μV/√Hz–20 μV/√Hz; *X axis* log format; 100 MHz–10 Hz)

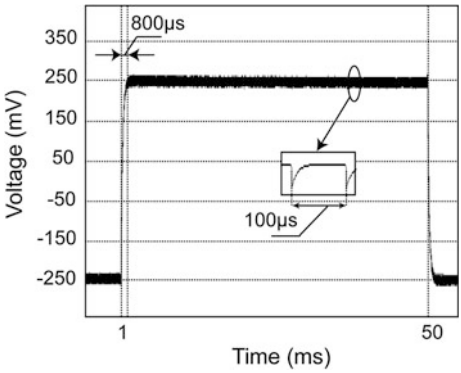

Fig. 7.25 Transient step response of the capacitively coupled instrumentation amplifier

settled well before the end of the clock phase so that a succeeding ADC could avoid the spikes by sampling just before the next clock transition.

For biopotential measurements, the DSL was turned on, resulting in the high-pass frequency response shown in Fig. 7.26. The high-pass corner frequency was located at 0.5 Hz. At frequencies below 100 Hz, the measured AC CMRR was larger than 110 dB, which is at least 30 dB higher than [17, 18]. The chip area with the DSL is 7× smaller than that of the fully differential version of its prior art [1]. However, the noise of the CCIA with the DSL increased to 6.7 μVrms in a bandwidth of 0.5–100 Hz for biosignals. The noise spectrum is shown in Fig. 7.27. It can be seen that the low-frequency noise dominates. This noise, which although it looks like 1/*f* noise, is the noise caused by the shot current noise of the input chopper in the VLT integrator. This current noise is converted into voltage by the input capacitors, and thus increases as the frequency decreases. A similar effect has been observed in several other biomedical IAs. A detailed explanation of this effect can be found in [25]. The key specifications of the CCIA are summarized by Table 7.2.

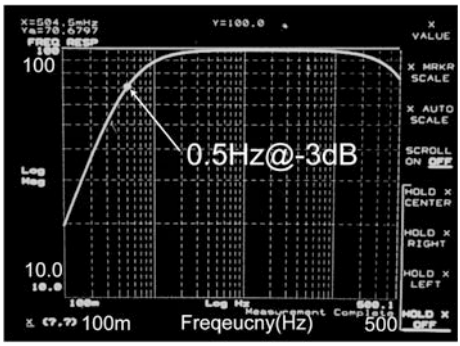

Fig. 7.26 High-pass response of the capacitively coupled instrumentation amplifier with the DC servo loop. (*Y axis* log format; 10–100; *X axis* log format; 100 MHz–500 Hz)

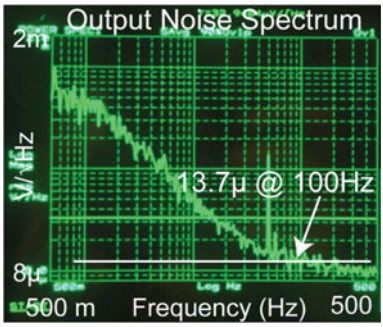

Fig. 7.27 Output noise spectrum of the CCIA in AC mode with a gain of 100 (*Y axis* log format; 8 μV/√Hz–2 mV/√Hz; *X axis* log format; 500 MHz–500 Hz)

Table 7.2 Performance summary

	DC mode	AC mode
Chopping frequency (kHz)	5	1.25
Offset	1 μV	N/A
Band-pass	N/A	0.5 Hz–700 Hz
Power (μW)	1.8	2.1
Area (mm^2)	0.1	0.2
CMVR	0 V−V_{DD}	0 V−V_{DD}
CMRR	>134 dB (DC)	>110 dB (100 Hz)
Technology (nm)	65	65
Input impedance	30 M ohm (DC)	80 M ohm (AC)
Input-referred noise	600 nVrms	6.7 μV

7.6 Conclusion

A precision CCIA has been implemented in a 65 nm CMOS technology. For DC measurements, it achieves state-of-the-art performance in terms of NEF, offset, CMRR, PSRR, and gain accuracy. The CCIA's power efficiency is high due to the use of a capacitively coupled chopper topology. It has a rail-to-rail DC CM input

range without using a rail-to-rail input stage. Since it operates from a 1 V supply, the power consumption of the amplifier is 1.8 μW with a chip area of 0.1 mm^2. With an additional DSL for AC measurements, the CCIA can be used for biopotential sensing, for which it consumes 2.1 μW power consumption and occupies a chip area of 0.2 mm^2. The deep submicron technology, low supply voltage, low power consumption, and small area make the CCIA suitable for a variety of wireless sensor applications.

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Chapter 8
Conclusions

In the previous chapters, the design and realization of prototype capacitively coupled chopper operational amplifiers (CCOPAs) and capacitively coupled chopper instrumentation amplifiers (CCIAs) have been described. In this chapter, conclusions will be drawn based on the experimental results obtained with these prototypes. The original contributions of the author are listed.

8.1 Conclusions

The theory and realizations presented in this thesis show that the combination of capacitive coupling and chopping can be successfully used to build both opamps (Chap. 5) and IAs (Chaps. 6 and 7) with a wide input common-mode voltage range (CMVR). In combination with the floating input chopper (Chap. 4), an input CMVR equal to the breakdown voltage of the input capacitors can be achieved, without any extra power consumption or a high voltage supply. Compared to other methods of expanding CMVR, this approach is not only much simpler, but is more power efficient. In particular, in the case of an IA, the capacitively coupled chopper topology confers not only low offset, low 1/*f* noise, and a high CMRR, but also higher power efficiency than the classic current-feedback and three-opamp topologies because it only requires one input differential pair. This makes such amplifiers especially well suited for use in precision wireless sensor nodes, where low power and low noise are both of critical importance. Due to the excellent matching of on-chip capacitors, high gain accuracy can also be obtained without the need for extra techniques such as dynamic element matching. The relatively low input impedance of a CCIA can be significantly increased by impedance boosting loops such as the one discussed in Chap. 7, while chopping ripple can be effectively suppressed by the area-efficient SC RRLs presented in Chaps. 5 and 7. Below is a

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Analog Circuits and Signal Processing, DOI 10.1007/978-3-319-47391-8_8

Table 8.1 Performance summary of the capacitively coupled chopper amplifiers presented in Chaps. 5, 6, and 7

	Chapter 5: CCOPA		Chapter 6: HV CCIA [3]	Chapter 7: LV CCIA (DC mode) [4]
	Multipath [1]	Single path [2]		
CMVR (V)	0 to 20	0 to 20	−30 to 30	0 to 1
CMRR (dB)	140	140	160	134
Power (μW)	40	50	78	2.1
Offset (μV)	3	3	5	1
Noise (nV/$\sqrt{\text{Hz}}$)	56	42	31	60
GBW	800 kHz	400 kHz	1 M	70 kHz
Gain accuracy	NA	NA	0.13 %	0.16 %

table showing the key performance of the designs presented in earlier chapters (Table 8.1).

Apart from the advantages such as wide CMVR, high DC CMRR, high power efficiency, and gain accuracy, capacitively coupled chopper amplifiers also have some drawbacks. As explained in Sect. 6.3.4, one major drawback of CCIAs is the presence of chopping spikes at their outputs. These can be reduced by reducing the value of the feedback capacitors, implementing a strong output stage, or by employing S&H filter at the output of the amplifier as explained in Sect. 6.3.4.

8.2 Original Contributions

- The invention of the capacitively coupled floating choppers (Chap. 4).
- The analysis and realization of the two above-the-rail CCOPA prototypes are described (Chap. 5).
- The analysis and realization of a beyond-the-rail CCIA for high/low-side current sensing are given (Chap. 6).
- The realization of a multipurpose low-voltage CCIA for wireless sensor nodes (Chap. 7).
- The demonstration of an input impedance boosting technique for CCIAs (Chap. 7).
- Two potential CCADC architectures have been suggested as a basis for future work (Chap. 8).

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